

METHOD 2010.14

INTERNAL VISUAL (MONOLITHIC)

1. PURPOSE. The purpose of this test is to check the internal materials, construction, and workmanship of microcircuits for compliance with the requirements of the applicable acquisition document. This test will normally be used prior to capping or encapsulation on a 100 percent inspection basis to detect and eliminate devices with internal defects that could lead to device failure in normal applications. It may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for microelectronic devices. Furthermore, the criteria of this test method will be used during destructive physical analysis (DPA) following the procedures outlined in test method 5009, "Destructive Physical Analysis". Test condition A and B provide a rigorous and detailed procedure for internal visual inspection of high reliability microcircuits as specified in the screening requirements of test method 5004. For condition B product the alternate screening procedure (alternate 1) documented in test method 5004 may be used by the manufacturer as an option to internal visual inspection as specified. For condition A or B product, the alternate screening procedure (alternate 2) documented in test method 5004 may be used by the manufacture as an option to internal visual inspection as specified.

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification and any visual standards (gauges, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

2.1 GaAs device requirements. GaAs devices shall be inspected to all applicable criteria as listed herein. GaAs microwave devices shall also have additional specific criteria as listed and the applicable high power magnification for individual features of GaAs microwave devices shall be selected from the following table.

TABLE I. GaAs microwave device high magnification requirements.

Feature Dimensions	Magnification range
> 5 microns	75 - 150x
1 - 5 microns	150 - 400x
< 1 micron	400 - 1000x

2.2 Silicon-on-Sapphire (SOS) device requirements. SOS devices shall be inspected to all applicable criteria specified herein, except where noted. The sapphire portions of the die shall be considered "nonconductive and nonoperational material".

3. PROCEDURE.

- a. General. The device shall be examined within the specified magnification range to determine compliance with the requirements of the applicable acquisition document and the criteria of the specified test condition.

The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device process or technology, it has been indicated.

- b. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer.

When inverted die mounting techniques are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to attachment of the die. Devices that fail any test criteria herein are defective devices and shall be rejected and removed at the time of observation.

Visual criteria may be inspected as follows:

- (1) Prior to die attachment without re-examination after die attachment; 3.1.1.2, 3.1.1.5, 3.1.1.7, 3.1.2, 3.1.4 e and f, 3.1.5, 3.1.6 a-f, 3.2.6.
  - (2) Prior to bonding without re-examination after bonding; 3.2.3.
  - (3) For condition B only; the following criteria may be inspected prior to die attachment at high power, plus low power after die attachment, provided a high magnification sample to sample size number = 45 accept number C = 0 is performed at precap inspection; 3.1.1.1, 3.1.1.3, 3.1.1.4, 3.1.1.6, 3.1.3, 3.1.4 a-d and g-o, 3.1.6 g and h, 3.1.7. If the sample fails the entire lot shall be reinspected at high magnification for the failed criteria.
- c. Inspection control. In all cases except die at incoming inspection, examination prior to final preseat inspection shall be performed under the same quality program that is required at the final preseat inspection station. Care shall be exercised after inspections in accordance with 3b, to insure that defects created during subsequent handling will be detected and rejected at final preseat inspection. During the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment. Devices examined to condition A shall be inspected and prepared for sealing in a Class 5 controlled environment and devices examined to condition B criteria shall be inspected and prepared for sealing in a Class 8 controlled environment (see A.4.8.1.1.7 of appendix A of MIL-PRF-38535), except that the maximum allowable relative humidity in either environment shall not exceed 65 percent. Devices shall be in covered containers when transferred from one controlled environment to another.
- d. Magnification. "High magnification" inspection shall be performed perpendicular to the die surface with the device under illumination perpendicular to the die surface. "Low magnification" inspection shall be performed with a metallurgical or stereomicroscope with the device under suitable illumination. Low magnification may be performed at an angle other than 90° to the die surface to facilitate the inspection. The inspection criteria of 3.2.1 may be examined at "high magnification" at the manufacturer's option.
- e. Reinspection. When inspection for product acceptance is conducted subsequent to the manufacturer's inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the acquisition document. When suspected defects or deficiencies are noted, additional inspection may be performed at magnifications needed to evaluate or resolve the suspect items.

f. Definitions:

- (1) Active circuit area. All areas enclosed by the perimeter of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.
- (2) Coupling (air) bridge. A raised layer of metallization used for interconnection that is isolated from the surface of the element.
- (3) Block resistor. A thin film resistor which for purposes of trimming is designed to be much wider than would be dictated by power density requirements and shall be identified in the approved manufacturer's precap visual implementation document.
- (4) Contact Via. The Via where dielectric material is etched away in order to expose the Under Bump Metalization (UBM) on the bond pads or solder bump attach pads.
- (5) Channel. An area lying between the drain and the source of FET structures.
- (6) Controlled environment (Clean Room). An environment maintained for humidity and atmospheric particle count in accordance with ISO 14644-1. A Class 5 controlled environment has no more than 100 (0.5  $\mu\text{m}$  or greater) particles/cubic-foot of air, a Class 6 controlled environment has no more than 1,000 (0.5  $\mu\text{m}$  or greater) particles/cubic-foot of air, and a Class 8 controlled environment has no more than 100,000 (0.5  $\mu\text{m}$  or greater) particles/cubic-foot of air, except that the maximum allowable relative humidity shall not exceed 65 percent.
- (7) Crazing. The presence of numerous minute cracks in the referenced material, (e.g., glassivation crazing).
- (8) Detritus. Fragments of original or laser modified resistor material remaining in the kerf.
- (9) Die Coat. A thin layer of soft polyimide coating applied to the surface of a semiconductor element that is intended to produce stress relief resulting from encapsulation and to protect the circuit from surface scratches.
- (10) Dielectric isolation. Electrical isolation of one or more elements of a monolithic semiconductor integrated circuit by surrounding the elements with an isolating barrier such as semiconductor oxide.
- (11) Dielectric layer or layers. Dielectric layer or layers deposited on the die surface to protect the redistribution metalization, and to create the contact via for solder bump pad.
- (12) Diffusion tub. A volume (or region) formed in a semiconductor material by a diffusion process (n- or p- type) and isolated from the surrounding semiconductor material by a n-p or p-n junction or by a dielectric material (dielectric isolation, coplanar process, SOS, SOI).
- (13) Foreign material. Any material that is foreign to the microcircuit or package, or any nonforeign material that is displaced from its original or intended position within the microcircuit package.
- (14) Functional circuit elements. Diodes, transistors, crossunders, capacitors, and resistors.
- (15) Gate oxide. The oxide or other dielectric that separates gate metallization (or other material used for the gate electrode) from the channel of MOS structures (see figure 2010-1).
- (16) Glassivation. The top layer(s) of transparent insulating material that covers the active circuit area, with the exception of bonding pad areas and beam leads.
- (17) Glassivation cracks. Fissures in the glassivation layer.

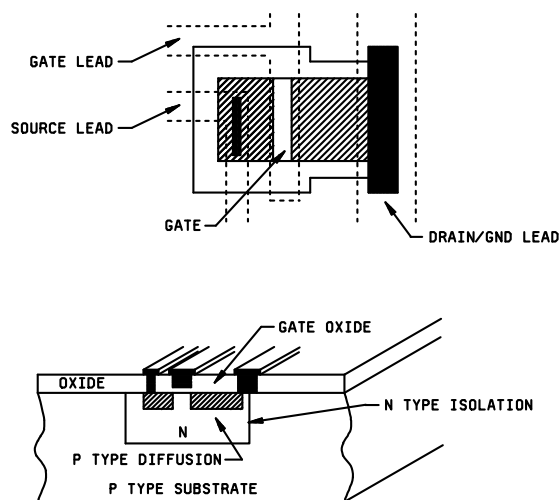


FIGURE 2010-1. P channel MOS transistor.

- (18) Junction line. The outer edge of a passivation step that delineates the boundary between "P" and "N" type semiconductor material. An active junction is any P/N junction intended to conduct current during normal operation of the circuit element, (e.g., collector to base).
- (19) Kerf. That portion of the component area from which material has been removed or modified by trimming or cutting.
- (20) Line of separation. Visible distance or space between two features that are observed not to touch at the magnification in use.
- (21) MESFET. (Metal semiconductor field-effect transistor). A field-effect transistor in which a metal semiconductor rectifying contact is used for the gate electrode. Typically the structure is fabricated in gallium arsenide and the term GaAs MESFET may be used. Both depletion-type and enhancement type devices have been manufactured. The acronyms are D-MESFET, and E-MESFET, respectively.
- (22) Metallization nonadherence. Unintentional separation of material from an underlying substrate excluding air bridges and undercutting by design.
- (23) Multilayered metallization (conductors). Two or more layers of metal or any other material used for interconnections that are not isolated from each other by insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal (see figure 2010-2).
- (24) Multilevel metallization (conductors). Two or more levels of metal or any other material used for interconnections that are isolated from each other by insulating material (also referred to as interlevel dielectric) (see figure 2010-3).
- (25) Narrowest resistor width. The narrowest portion of a given resistor prior to trimming.

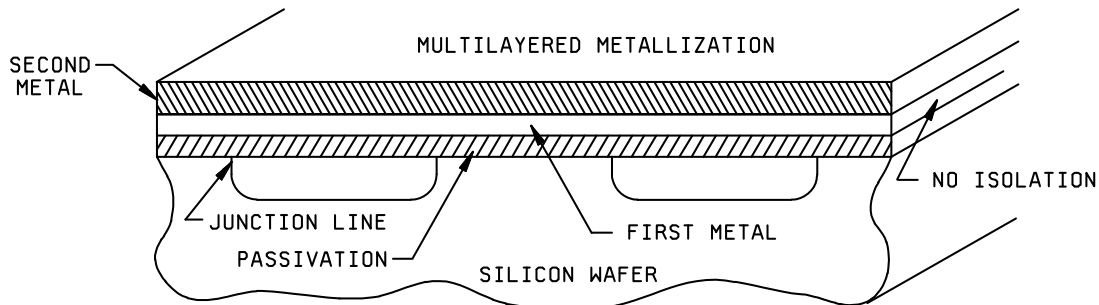


FIGURE 2010-2. Multilayered metallization.

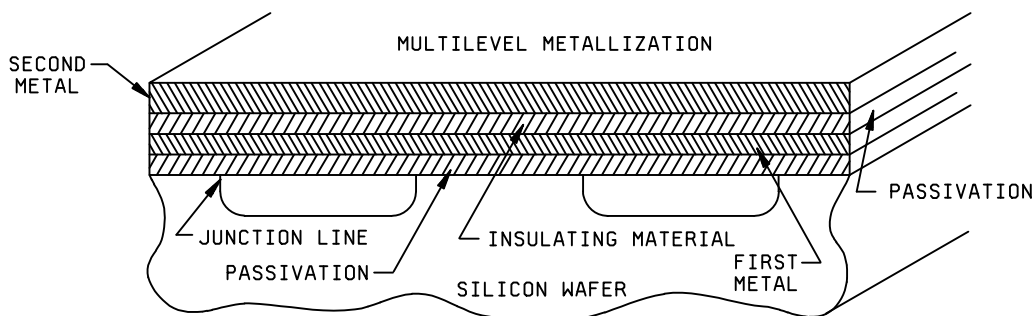


FIGURE 2010-3. Multilevel metallization.

- (26) Operating metallization (conductors). Metal or any other material used for interconnection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings.
- (27) Original width. The width dimension or distance that would have been present, in the absence of the observed abnormality (e.g., original metal width, original diffusion width, original beam width, etc.).
- (28) Package post. A generic term used to describe the bonding location on the package.
- (29) Passivation. The silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal or between metal levels on multilevel devices.
- (30) Passivation step. An abrupt change of elevation (level) of the passivation such as a contact window, or operating metallization crossover.

- (31) Peripheral metal. All metal that lies immediately adjacent to or over the scribe grid.
  - (32) Redistribution Layer (RDL). Layer added to original wafer/die surface to allow for the redistribution of bond pads into a format more suitable to flip chip.
  - (33) Redistribution metalization. The metal deposited on the RDL to create the electrical conductors which connect the original bond pads to the distributed solder bump pads.
  - (34) Shooting metal. Metal (e.g., aluminum, gold) expulsion of various shapes and lengths from under the wire bond at the bonding pad.
  - (35) Solder ball. Solder ball or sphere attached to the UBM through the contact via after a re-flow process.
  - (36) Solder Bump. Solder that is either electroplated or screened into the photo resist opening. After the photo resist is removed the solder resembles a bump before it is reflowed into ball or sphere.
  - (37) Substrate. The supporting structural material into or upon which or both the passivation, metallization and circuit elements are placed.
  - (38) Substrate via. A small hole formed through the wafer and metallized, causing electrical connection to be made from the frontside (the side on which the circuitry is formed) to the backside of the wafer.
  - (39) Thick film. That conductive/resistive/dielectric system that is a film having greater than 50,000Å thickness.
  - (40) Thin film. That conductive/resistive/dielectric system that is a film equal to or less than 50,000Å in thickness.
  - (41) Under Bump Metalization (UBM). Metals deposited on top of the aluminum bond pads or on the solder bump pads that enhance wetting and protect against intermetallic reactions between the solder and the original metal on the pads.
  - (42) Via metallization. That which connects the metallization of one level to another.
- g. Interpretations. Reference herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used for confirming that a reject condition does not exist, they shall be approved by the acquiring activity. For inspections performed on the range of 75X to 100X, the criteria of 0.1 mil of passivation, separation or metal can be satisfied by a line of separation or a line of metal visible.
- h. Foreign material control. The manufacturer shall perform an audit on a weekly basis for (1) the presence of foreign material within incoming piece part lids and bases, and (2) the presence of foreign material on the die surface or within the package of assembled parts.

The audit of assembled parts may be satisfied during routine internal visual inspection. If the presence of foreign material is discovered, the manufacturer shall perform the necessary analysis on a sample of the foreign material on the suspect devices to determine the nature of the material. The manufacturer shall document the results of this investigation and corrective action to eliminate the foreign material and this information will be available to the Government QAR, and the acquiring activity or the qualifying activity, as applicable. A corrective action plan shall be obtained within a maximum of 10 working days of discovery.

The audit of incoming piece part lids and bases shall be performed before parts are assembled, or may be satisfied during routine incoming quality inspection. If the presence of foreign material of a size 1 mil or greater is discovered, the manufacturer will analyze the foreign material to determine its nature and document the results of the analysis. If applicable, these results shall be distributed to the vendor supplying the parts, with the request that the vendor document corrective actions to minimize or eliminate such foreign material. This information will be available to the manufacturer, Government QAR, and the acquiring activity or qualifying activity, as applicable.

NOTE: The piece part audit requirements can be replaced by a piece part cleaning process, approved by the qualifying activity, that is always performed either prior to or during the assembly process and these piece parts are stored in a controlled environment until they are used.

The intent of these procedures is to require investigation and resolution of foreign material problems that do not have an effective screening or detection methodology but that could cause degradation and eventual failure of the device function. Repetitive findings without obvious improvements require escalation to Director of Manufacturing and Director of Quality Assurance to continue processing.

Condition A  
Class level S

Condition B  
Class level B

3.1 High power inspection. Internal visual examination as required in 3.1.1 through 3.1.3 shall be conducted on each microcircuit. In addition, the applicable criteria contained in 3.1.4 through 3.1.7 shall be used for the appropriate microcircuit area where glassivation, dielectric isolation or film resistors are used.

NOTE: Unless otherwise specified, for flip chip product the criteria of 3.1 shall apply only to top circuit side inspection. After die mounting, only criteria in 3.1.3i shall apply.

The high magnification inspection shall be within the range of 100X to 200X.

The high magnification inspection shall be within the range of 75X to 150X.

For high magnification inspection of GaAs microwave devices, see table I herein. Also, for < 1 micron features, the manufacturer may implement a sample inspection plan which shall be documented in the manufacturer's internal procedure and approved by the qualifying activity.

3.1.1 Metallization defects. No device shall be acceptable that exhibits the following defects in the operating metallization.

3.1.1.1 Metallization scratches:

- a. Scratch in the metallization excluding bonding pads and beam leads that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-4).
- a. Scratch in the metallization, excluding bonding pads and beam leads, that exposes underlying passivation anywhere along its length and leaves less than 50 percent of the original metal width undisturbed (see figure 2010-5).

NOTE: For GaAs microwave devices, scratches in the gate stripe or gate insertion metallization.

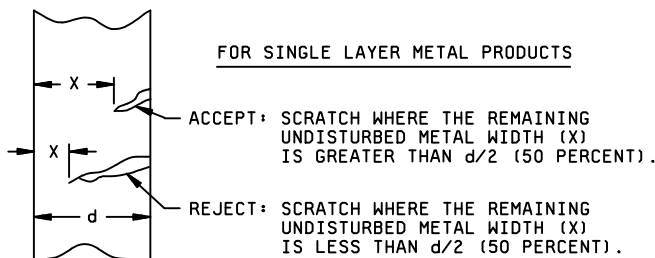


FIGURE 2010-4. Metallization scratch criteria for class level S.

Condition A  
Class level S

Condition B  
Class level B

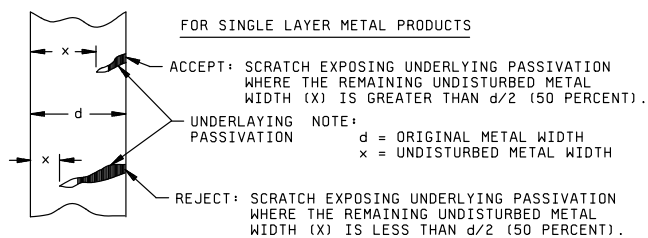
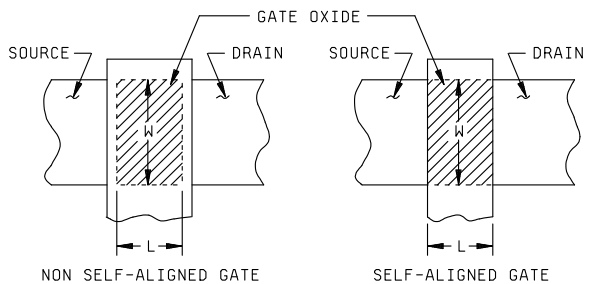


FIGURE 2010-5. Metallization scratch criteria for class level B.

b. For condition A, see 3.1.1.1a above.

b. For condition B only. Scratch that completely crosses a metallization path and damages the surface of the surrounding passivation, glassivation, or substrate on either side (for MOS devices, the path shall be the (L) dimension) (see figure 2010-6).



NOTE: When standard metallization scratch criterion is applied to the gate area, the dimensions (W) and (L) shall be considered as the original channel width and length respectively.

FIGURE 2010-6. MOS scratch criteria.



Condition A  
Class level S

Condition B  
Class level B

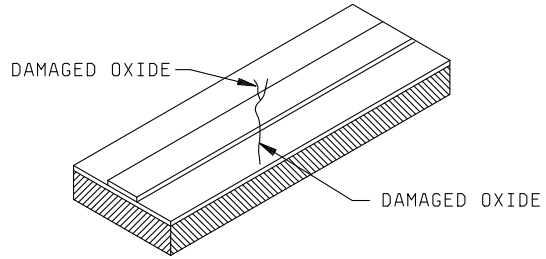


FIGURE 2010-6. MOS scratch criteria - Continued.

- c. Scratch in multilayered metallization, excluding bonding pads and beam leads that exposes underlying metal or passivation anywhere along its length and leaves less than 75 percent of the original metal width undisturbed (see figure 2010-7).

- c. Scratch in multilayered metallization, excluding bond pads and beam leads that exposes the underlying metal anywhere along its length and leaves less than 25 percent of the original metal width undisturbed (see figure 2010-8).

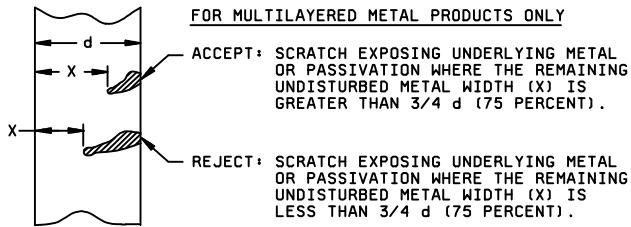


FIGURE 2010-7. Scratch criteria for class level S.

Condition A  
Class level S

Condition B  
Class level B

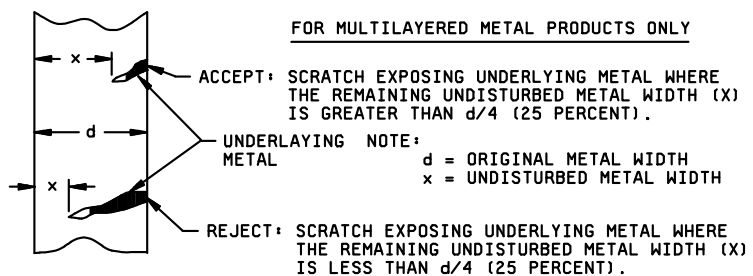


FIGURE 2010-8 Scratch criteria for class level B.

NOTE: For condition B only. Criteria 3.1.1.1a, b, and c can be excluded for peripheral power or ground metallization where parallel paths exist such that an open at the scratch would not cause an unintended isolation of the metallization path.

- d. Scratch in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: For condition B only. Criteria 3.1.1.1a, b, c, and d can be excluded for the last 25 percent of the linear length of the contact cut and all metal beyond, on the termination end(s) of the metallization runs. In these cases there shall be at least 50 percent of the contact opening area covered by metallization and at least a continuous 40 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-9).

Condition A  
Class level S

Condition B  
Class level B

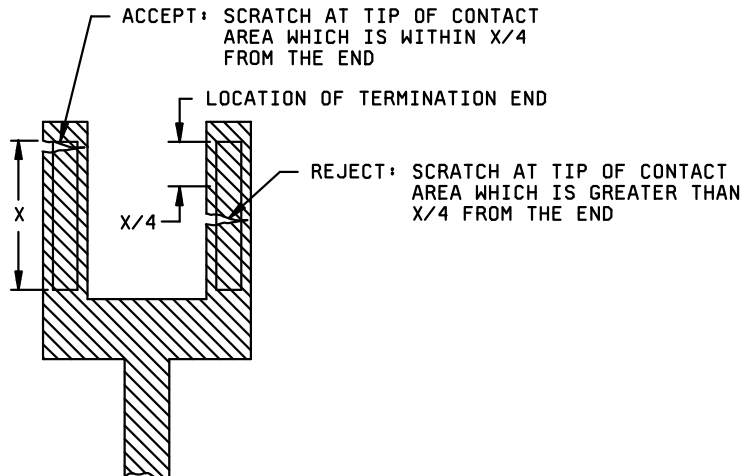


FIGURE 2010-9. Termination ends.

e. Scratch in the metallization, over the gate oxide (applicable to MOS structures only) (see figure 2010-10).

e. Scratch in the metallization, over the gate oxide, that exposes underlying passivation and leaves less than 50 percent of the length or width of the metallization between source and drain diffusion undisturbed (applicable to MOS structures only) (see figure 2010-11).

Condition A  
Class level S

Condition B  
Class level B

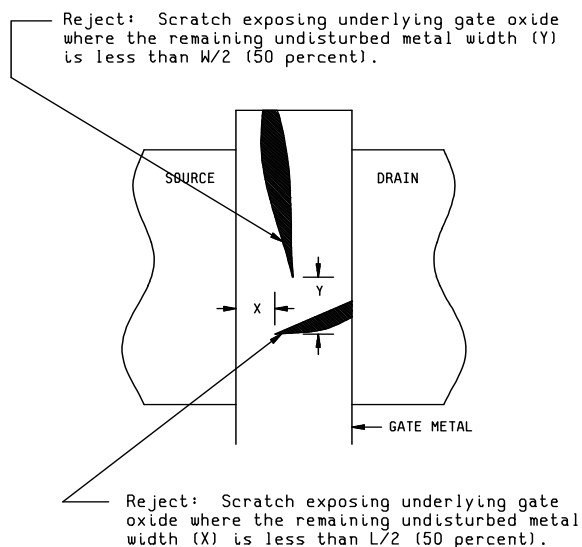
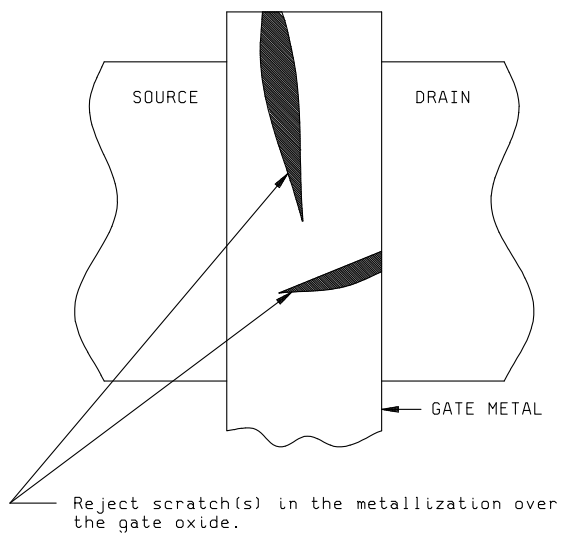


FIGURE 2010-10. MOS scratch criteria for class level S.

FIGURE 2010-11. MOS scratch criteria for class level B.

Condition A  
Class level S

Condition B  
Class level B

- f. Scratch in the metallization that exposes the dielectric material of a thin film capacitor or crossover. (Not applicable to air bridges.)
- g. Scratch in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.
- h. Scratch(es) (probe mark(s), etc.) in the bonding pad area that exposes underlying passivation, or substrate, and leaves less than 75 percent of the unglassivated metallization area undisturbed.
- i. For GaAs devices only, any tears, peeling, gaps, and lateral displacement of metal.

3.1.1.2 Metallization voids:

- a. Void(s) in the metallization that leaves less than 75 percent of the original metal width undisturbed (see figure 2010-12).

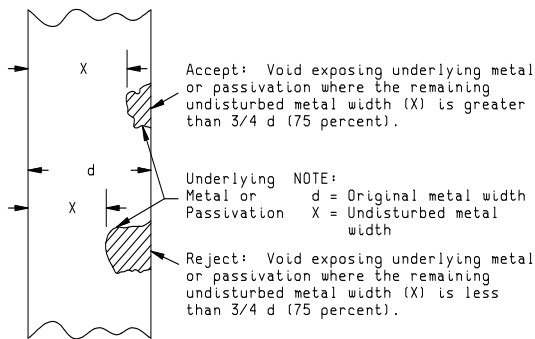


FIGURE 2010-12. Void criteria for class level S.

- a. Void(s) in the metallization that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-13).

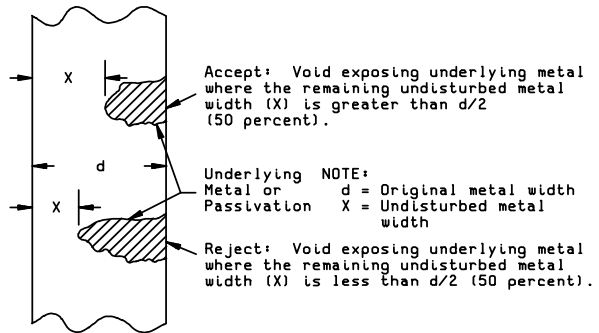


FIGURE 2010-13. Void criteria for class level B.

NOTE: For condition B only. Criteria can be excluded for peripheral power or ground metallization where parallel paths exist so that an open at the void(s) would not cause an unintended isolation of the metallization path.

Condition A  
Class level S

Condition B  
Class level B

- b. Void(s) in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: For condition B only. Criteria of 3.1.1.2a and b can be excluded for the last 25 percent of the linear length of the contact cut and all metal beyond on the termination end(s) of metallization runs. In these cases there shall be at least 50 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-14).

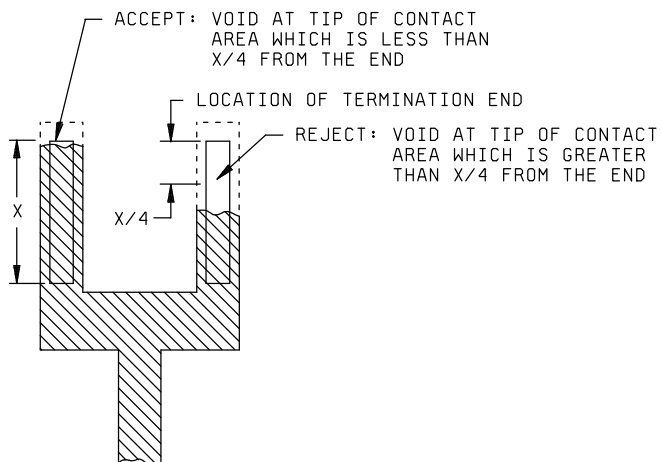


FIGURE 2010-14. Termination ends.

- c. Void(s) in the metallization over the gate oxide that leaves less than 75 percent of the metallization length (L) or width (W) between source and drain diffusions undisturbed (applicable to MOS structures only) (see figure 2010-15).

Condition A  
Class level S

Condition B  
Class level B

- d. Void(s) that leave less than 75 percent of the metallization area over the gate oxide undisturbed (applicable to MOS structures only).
- e. Void(s) that leaves less than 75 percent of the metallization width coincident with the source or drain diffusion junction line undisturbed (applicable to MOS structures only) (see figure 2010-15).

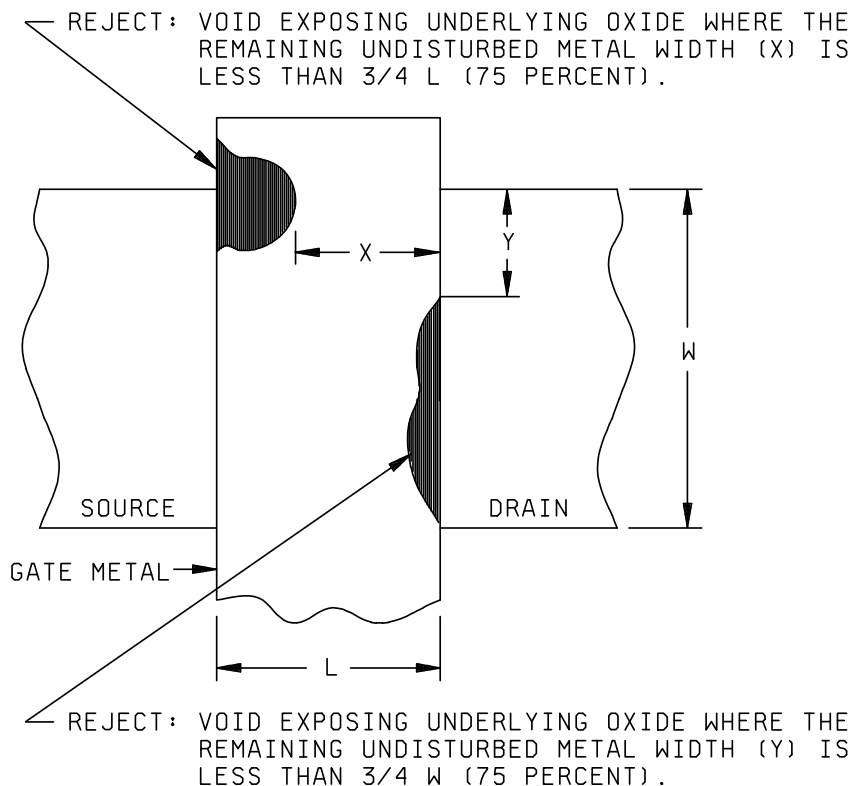


FIGURE 2010-15. MOS void criteria.

- f. Void(s) in the bonding pad area that leaves less than 75 percent of its original unglassivated metallization area undisturbed (see figure 2010-16).
- g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 75 percent of the narrowest entering metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately. (see figure 2010-16).
- g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately (see figure 2010-16).

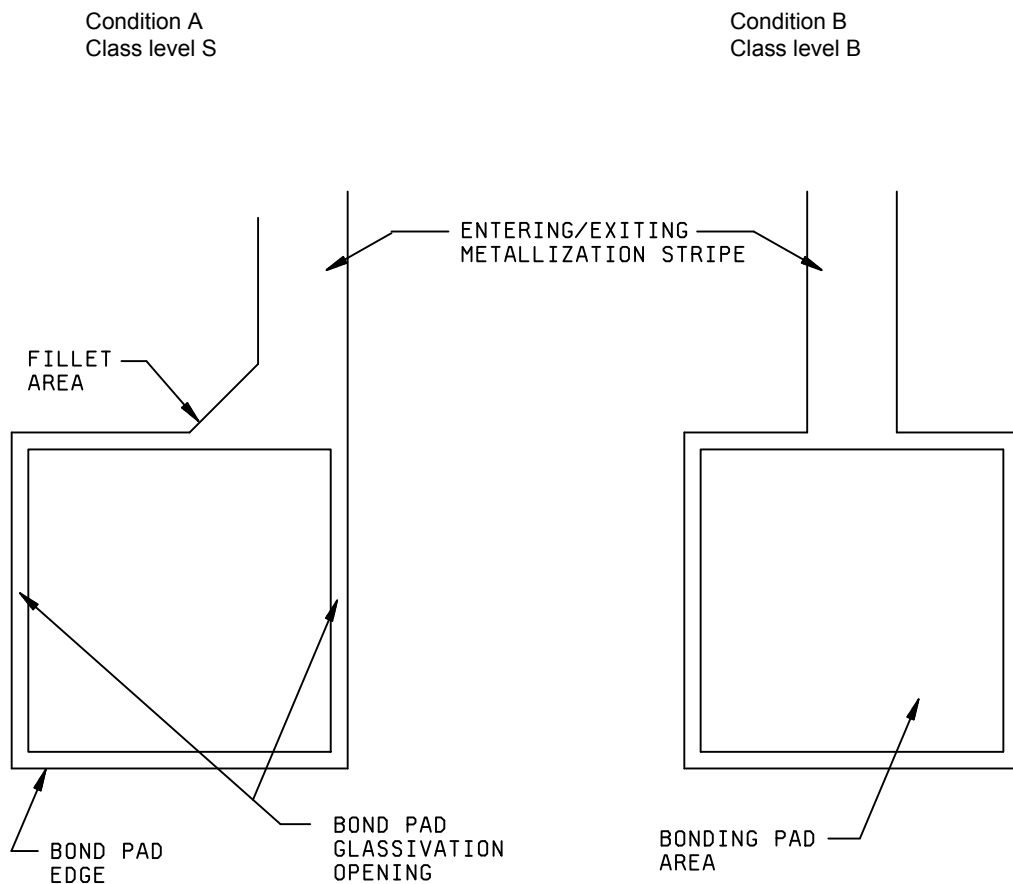


FIGURE 2010-16. Bond pad terminology.

NOTE: When a fillet area exists, it is to be considered as part of the entering/exiting metallization stripe.

- h. Void(s) in the metallization area of a thin film capacitor that leave less than 75 percent of the designed metallization area.
- i. For GaAs microwave devices only, voids in the gate stripe.

3.1.1.3 Metallization corrosion. Any metallization corrosion. Metallization having any localized discolored area shall be closely examined and rejected, unless it is demonstrated to be a harmless film, glassivation interface, or other obscuring effect.

3.1.1.4 Metallization nonadherence. Any metallization lifting, peeling, or blistering.

3.1.1.5 Metallization probing. Criteria contained in 3.1.1.1 shall apply as limitations on probing damage.



Condition A  
Class level S

Condition B  
Class level B

3.1.1.6 Metallization bridging.

NOTE: For SOS devices, exclude the insulator scribe lines.

- a. Any metallization bridging where the separation between metallization paths is reduced to less than 50 percent of the original design.
- b. Any metal that is displaced, as a result of bonding, from its original position on the bonding pad (shooting metal) greater than 1.0 mils or that reduces the separation between unglassivated operating metallization or scribe line and the bonding pad to less than 0.25 mils or 50 percent design separation, whichever is less.

- a. Any metallization bridging where a line of separation is not visible between metallization paths.

NOTE: For GaAs microwave devices, metallization bridging across spacings of less than 1  $\mu\text{m}$  shall be inspected only in accordance with 3.2 and table I at 400X to 1,000X. If a clear line of separation is not discernible, device functional testing at the wafer level shall suffice.

- b. Any metal that is displaced, as a result of bonding, from its original position on the bonding pad (shooting metal) that reduces the separation between unglassivated operating metallization or scribe line and the bonding pad such that a line of separation is not visible.

3.1.1.7 Metallization alignment.

- a. Contact window that has less than 75 percent of its area covered by metallization.
- b. Contact window that has less than a continuous 50 percent of its perimeter covered by metallization.
- c. Contact window that has less than 75 percent of its perimeter on two adjacent sides covered by metallization (applicable to MOS structures only).

- a. Contact window that has less than 50 percent of its area covered by metallization.
- b. Contact window that has less than 40 percent of its perimeter covered by metallization.

NOTE: When, by design, metal is completely contained in a contact window or does not cover the entire contact perimeter, criteria 3.1.1.7a, b, or c can be deleted, provided the design criteria is satisfied.

- d. A metallization path not intended to cover a contact window that is not separated from the contact window by a line of separation.
- e. Any exposure of the gate oxide (i.e., oxide not covered by gate electrode in the area between source and drain diffusions, applicable to MOS structures only) (see figure 2010-17).

3.1.1.8 Via hole metallization. For GaAs devices only,

- a. Overetched via hole or misaligned via visible around the pad.
- b. Poor adhesion (lifting, peeling or blistering).
- c. Any cracks originating at the via hole.
- d. Evidence of bulging metal over a via hole.
- e. Evidence of solder coming up through via hole pad, when die is mounted on a carrier.

Condition A  
Class level S

Condition B  
Class level B

3.1.1.9 Coupling (air) bridge defects "high magnification". For GaAs devices only. No element shall be acceptable that exhibits:

- a. A void in the coupling (air) bridge metallization that leaves less than 75 percent of the original metallization width undisturbed. (see figure 2010-17A).
- b. Nodules or bumps that are greater, in any dimension, than the original coupling (air) bridge metallization width. (See figure 2010-17A)
- c. Coupling (air) bridge that contacts underlying operating metallization. (See figure 2010-17A)
- d. Attached, conductive foreign material that is greater, in any dimensions, than 50% of the original coupling (air) bridge metallization width.
- e. No visible separation between the coupling (air) bridge and the underlying operating metallization.

NOTE: This criterion is not applicable when an insulating material is used between the coupling (air) bridge and the underlying metallization. (See figure 2010-17A)

- f. Coupling (air) bridge metallization overhang over adjacent operating metallization, not intended by design, that does not exhibit a visible separation. (See figure 2010-17A)
- g. Mechanical damage to a coupling (air) bridge that results in depression (lowering) of coupling (air) bridge metallization over underlying operating metallization.

NOTE: Air bridges which are depressed, over operating metallization, due to normal backside processing are not considered mechanically damaged. A visual line of separation still applies in accordance with 3.1.1.9e.

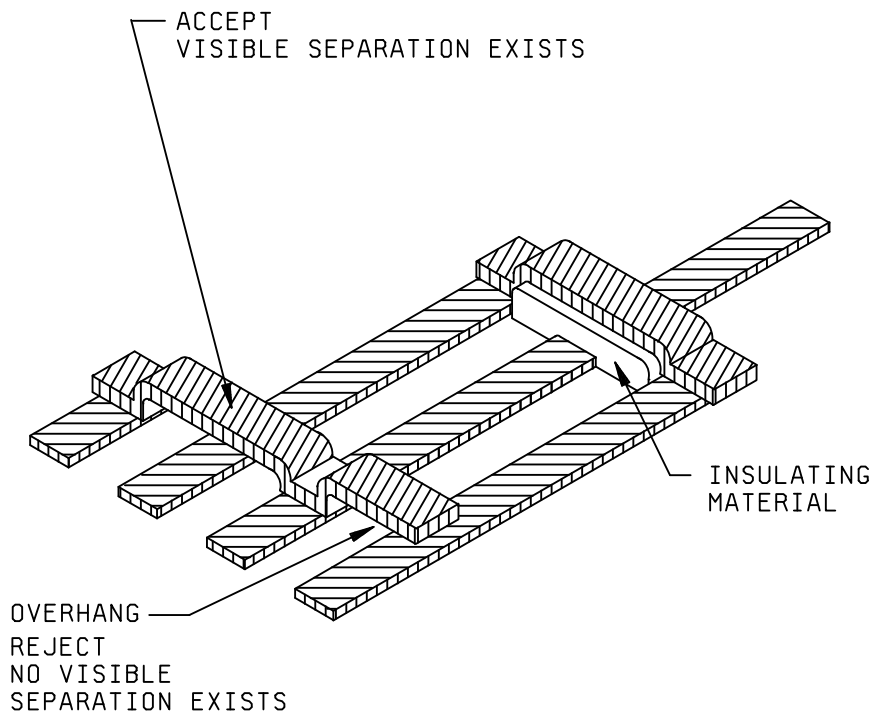
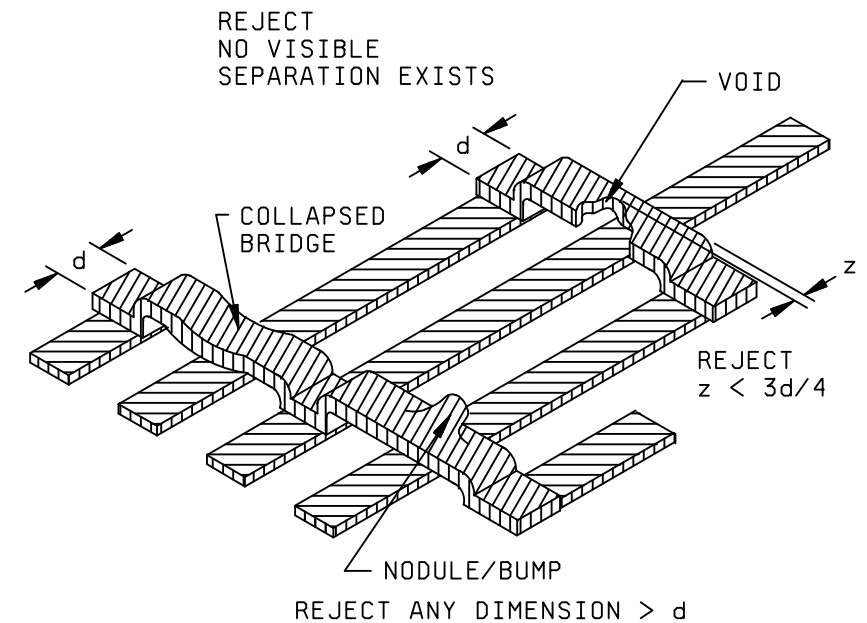


FIGURE 2010-17A. Class level S and Class level B coupling (air) bridge criteria.

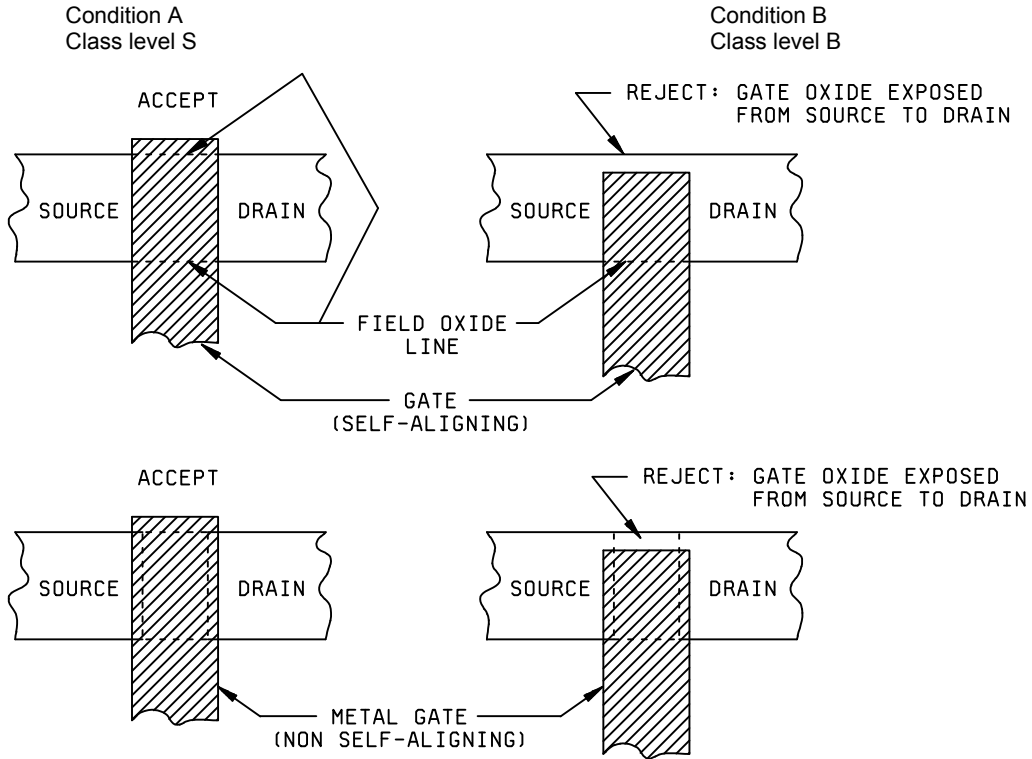


FIGURE 2010-17. MOS gate alignment.

- h. For MOS structures containing a diffused guard ring, gate metallization not coincident with or not extending over the diffused guard ring (see figure 2010-18).

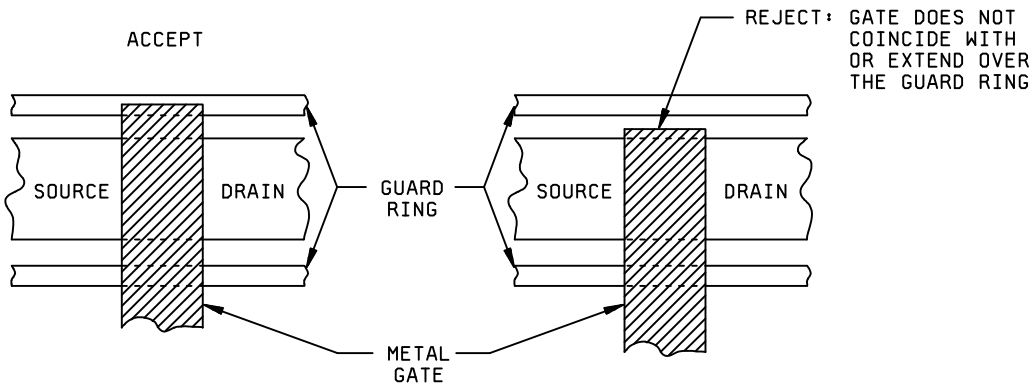


FIGURE 2010-18. MOS gate alignment.

Condition A  
Class level S

Condition B  
Class level B

3.1.2 Diffusion and passivation layer faults. No devices shall be acceptable that exhibits the following:

3.1.2.1 Diffusion faults.

- a. Diffusion fault that allows bridging between diffused areas (see figure 2010-19).

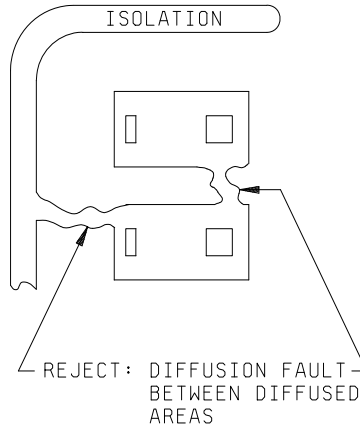


FIGURE 2010-19. Diffusion faults.

- b. Any isolation diffusion that is discontinuous (except isolation walls around unused areas or unused bonding pads) or any other diffused area with less than 25 percent (50 percent for resistors) of the original diffusion width remaining (see figure 2010-20).

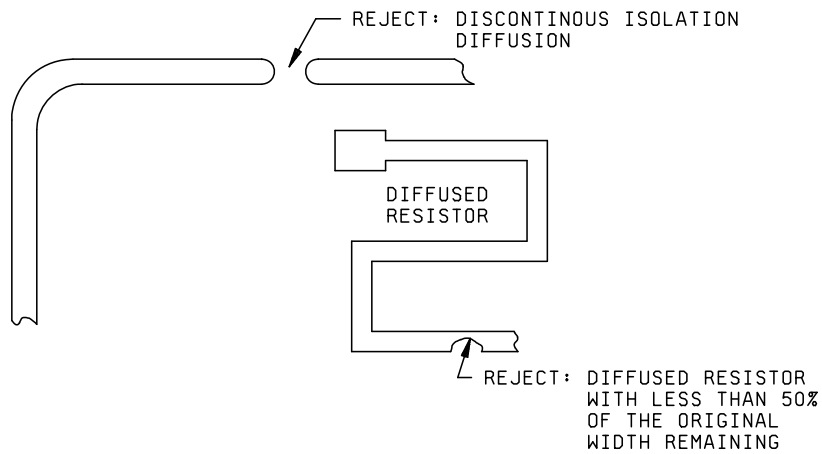


FIGURE 2010-20. Diffusion faults.

Condition A  
Class level S

Condition B  
Class level B

3.1.2.2 Passivation faults.

NOTE: For SOS devices, exclude defects between first-level conductive interconnect (metallization, polysilicon, ect.) and sapphire areas of the die, where no active circuit elements are present.

- a. Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization unless by design for GaAs devices. Multiple lines indicate that the fault can have sufficient depth to penetrate down to bare semiconductor material.

NOTE: The multiple line criteria can be excluded when a second passivation layer is applied in a separate operation prior to metallization deposition or for bond pads located in isolated tubs.

NOTE: For condition B only. Should the absence of glassivation in the defect area or the characteristics of the glassivation present allow verification of the presence or absence of passivation by color or color comparisons respectively, then these techniques may be used (see figure 2010-21).

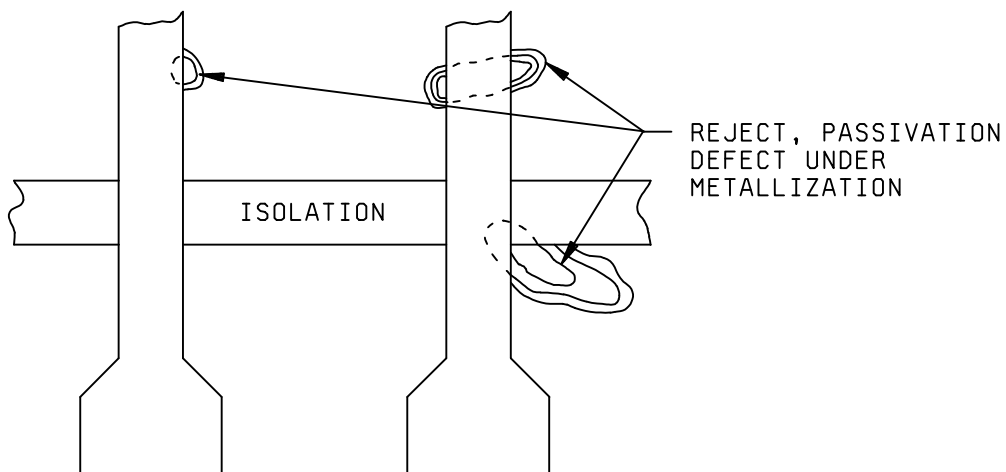


FIGURE 2010-21. Passivation faults.

- b. Active junction line not covered by passivation, unless by design.
- c. Contact window that extends across a junction line, unless by design.

Condition A  
Class level S

Condition B  
Class level B

3.1.3 Scribing and die defects. No device shall be acceptable that exhibits:

- |                                                                                                                                                      |                                                                                                                                  |
|------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| a. Less than 0.25 mil of passivation visible between operating metallization or bond periphery and bare semiconductor material (see figure 2010-22). | a. No line of separation between operating metallization or bond periphery and bare semiconductor material (see figure 2010-22). |
|------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|

NOTE: For GaAs devices only, less than 0.1 mil of substrate visible between operating metallization or bond periphery and edge of the die.

NOTE: Criteria can be excluded for beam leads and peripheral metallization including bonding pads where the metallization is at the same potential as the substrate.

NOTE: Does not apply to SOS devices.

- b. A chipout or crack in the active circuit area (see figures 2010-22 and 2010-38). In addition for GaAs a chipout into or underneath the functional metallization, e.g., bond pads, capacitors, peripheral metallization, etc., but excluding test structures of the device.

NOTE: Criteria can be excluded for peripheral metallization that is at the same potential as the substrate. At least 50 percent undisturbed metallization width shall remain at the chipout.

- |                                                                                                                                                                                                                 |                                                                                                                                                                                                                             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| c. A crack that exceeds 3.0 mils in length, or comes closer than 0.25 mils to any operating metallization (except for substrate potential peripheral metal) or functional circuit element (see figure 2010-22). | c. A crack that exceed 5.0 mils in length, or that does not exhibit a line of separation to any operating metallization (except for substrate potential peripheral metal) or function circuit element (see figure 2010-22). |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

- |                                                                                                                                                                                                                                                                                                 |                    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| d. For condition A only. Semicircular crack(s) terminating at the die edge, whose chord is long enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.) (see figure 2010-22). | d. No condition B. |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|

- e. Exposed semiconductor material extending over the passivation edge at the point of the beam lead exit from the die (applicable to beam lead structures only) (see figure 2010-38).

- f. Die having attached portions of the active circuit area of another die.

- g. A crack that exceeds 1.0 mil in length inside the scribe line (or semiconductor material edge for beam lead devices) that points toward operating metallization or functional circuit elements (see figure 2010-22).

- h. A crack that comes closer than 0.5 mil to operating beam lead metallization (see figure 2010-38).

NOTE: Criteria of 3.1.3c and h can be excluded for beam lead devices where the chipout or crack does not extend into the semiconductor material.

NOTE: Criteria of 3.1.3e and h do not apply to GaAs devices.

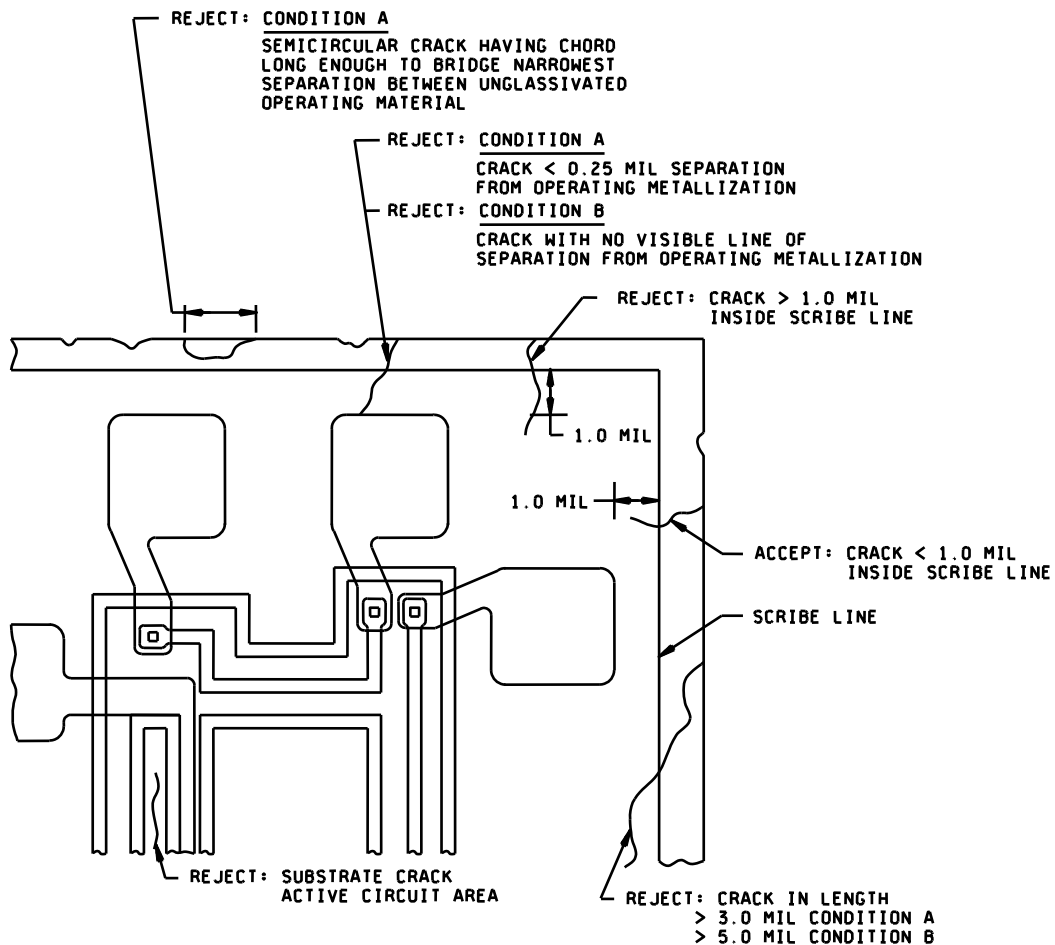


FIGURE 2010-22 Scribing and die defects.



Condition A  
Class level S

Condition B  
Class level B

- i. For flip chip, cracks, or chipouts in the substrate material that extends beyond 50 percent of substrate thickness or a crack greater than 5.0 mils in length in the substrate material (see figure 2010-23).

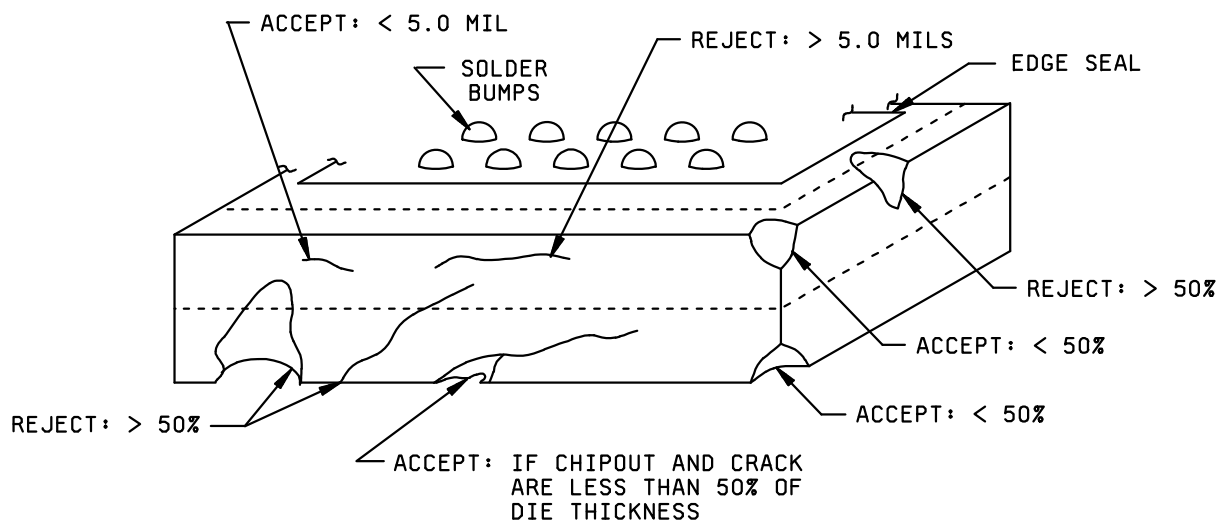


FIGURE 2010-23. Scribing and die defects.

- j. Any blistering, peeling, delamination, corrosion, or other gross defects in glassivation, metal, interlevel dielectrics or other layers.

Condition A  
Class level S

Condition B  
Class level B

3.1.4 Glassivation defects. No device shall be acceptable that exhibits (see figure 2010-24):

NOTE: For condition B only. Criteria of 3.1.4 can be excluded when the defect(s) is due to laser trimming. In this case, the defects outside the kerf due to laser trimming shall not be more than one half the remaining resistor width and shall leave a primary resistor path free of glassivation defects, equal to or greater than one half times the narrowest resistor width.

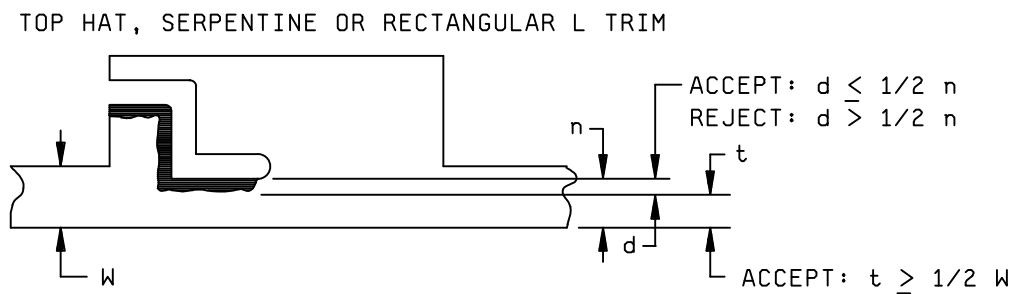


FIGURE 2010-24. Laser trimmed glassivation defects.

- Glass crazing or glass damage that prohibits the detection of visual criteria contained herein.
- Any lifting or peeling of the glassivation in the active areas or which extends more than 1.0 mil distance from the designed periphery of the glassivation.
- A glassivation void that exposes two or more active metallization paths, except by design.
- Unglassivated areas greater than 5.0 mils in any dimension, unless by design.
- Unglassivated areas at the edge of bonding pad exposing bare semiconductor material, except by design.
- Glassivation covering more than 25 percent of the designed open contact bonding area.
- Crazing over a film resistor.

Condition A  
Class level S

Condition B  
Class level B

- h. Scratch(es) in the glassivation that disturbs metal and bridges metallization paths.
- i. Crack(s) (not crazing) in the glassivation that forms a closed loop over adjacent metallization paths.
- j. Glassivation void(s) that exposes any portion of a thin film resistor or fusible link except where the glassivation is opened by design.
- k. For GaAs devices, voids in the glassivation that extends over the gate channel of the FET.
- l. For GaAs devices, scratches in the glassivation over the gate channel of the FET.
- m. For GaAs devices, scratches in the glassivation over the gate insertion of the FET.
- n. For GaAs devices, cracks in the glassivation which are more than 1.0 mil inside the scribe line, or are more than 50 percent of the distance between the scribe line and any functional or active element (e.g., capacitor, resistor, FET) and which point toward any functional or active element unless the crack terminates at a device feature (e.g., transmission line or dc line).

3.1.5 Dielectric isolation. No device shall be acceptable that exhibits:

- a. A discontinuous isolation line (typically a black line) around each diffusion tub containing functional circuit elements (see figure 2010-25).
- b. Absence of a continuous isolation line between any adjacent tubs, containing functional circuit elements (see figure 2010-25).

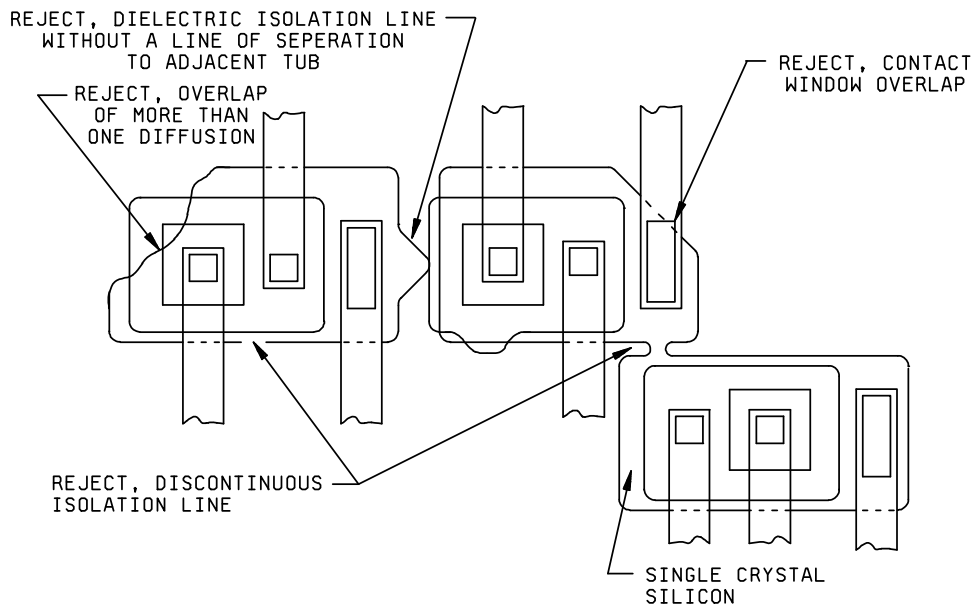


FIGURE 2010-25. Dielectric isolation defects.

Condition A  
Class level S

Condition B  
Class level B

- c. A diffused area which overlaps dielectric isolation material and does not exhibit a line of separation to an adjacent tub, or an overlap of more than one diffusion area into the dielectric isolation material (see figure 2010-25).

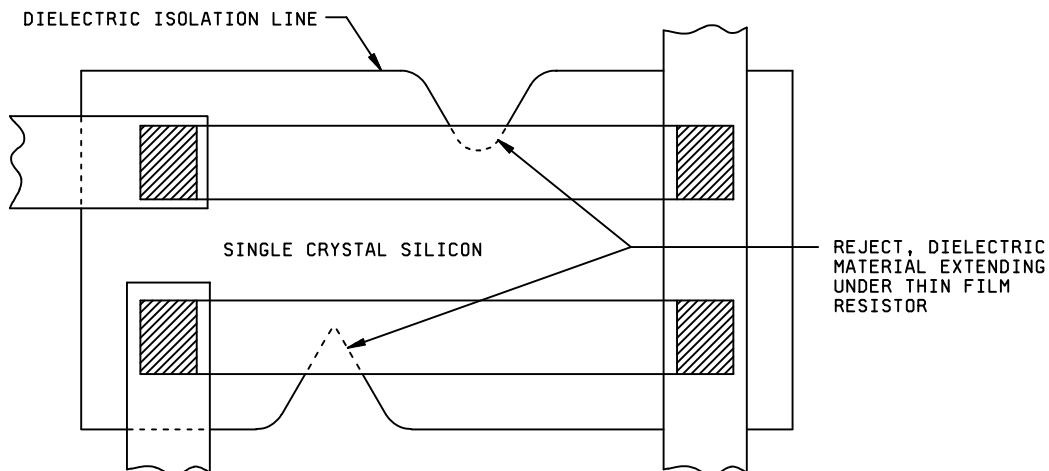


FIGURE 2010-26. Dielectric isolation defects.

- d. A contact window that touches or overlaps dielectric material, except by design.

NOTE: Metallization scratch and void defects over a dielectric isolation step shall be rejected in accordance with criteria contained in 3.1.1.1d and 3.1.1.2b.

3.1.6 Film resistor. Rejection shall be based on defects found within the actively used portions of the film resistor. Metallization defect criteria of 3.1.1 shall apply as applicable. No device shall be acceptable that exhibits:

Condition A  
Class level S

Condition B  
Class level B

- a. Any misalignment between the conductor/resistor in which the actual width  $X$  of the overlap is less than 50 percent of the original resistor width.

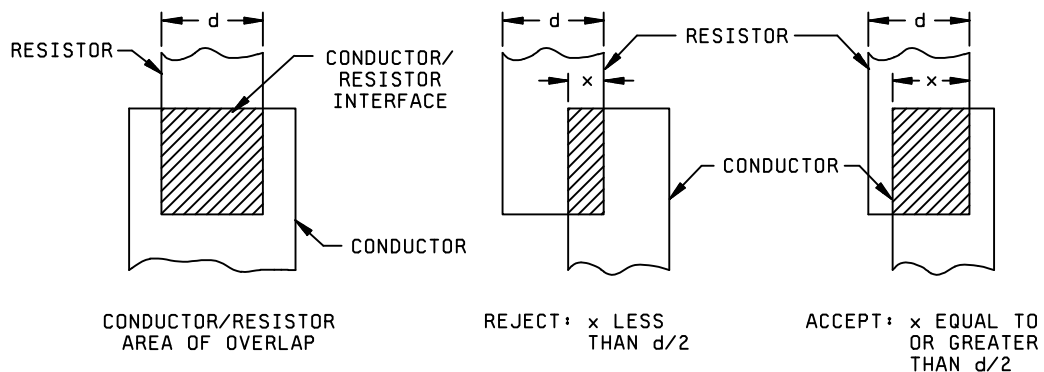


FIGURE 2010-27. Film resistor contact area.

- b. No visible line of contact overlap between the metallization and film resistor (see figure 2010-28).

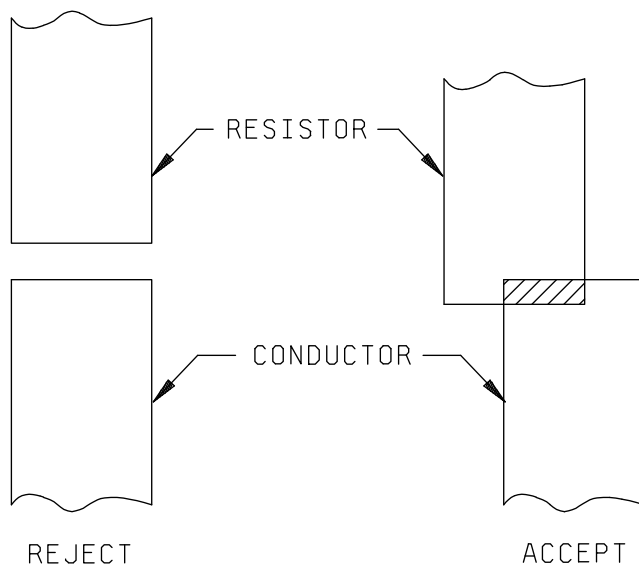


FIGURE 2010-28. Film resistor contact area.

Condition A  
Class level S

Condition B  
Class level B

- c. Void or necking down that leaves less than 75 percent of the film resistor width undisturbed at a terminal.
- d. Inactive resistor inadvertently connected to two separate points on an active circuit.
- e. Separation between any two resistors or a resistor and a metallization path that is less than 0.25 mil, or 50 percent of the design separation, whichever is less.
- f. Any thin film resistor that crosses a substrate irregularity (e.g., dielectric isolation line, oxide/diffusion step, etc.) (see figure 2010-26).

NOTE: This criteria does not apply to square isolated islands of single crystal silicon in the polysilicon area.

- g. Any resistor width reduced to less than one half the narrowest resistor width, resulting from voids or scratches or a combination thereof (see figure 2010-29).

NOTE: Maximum allowable current density requirements shall not be exceeded.

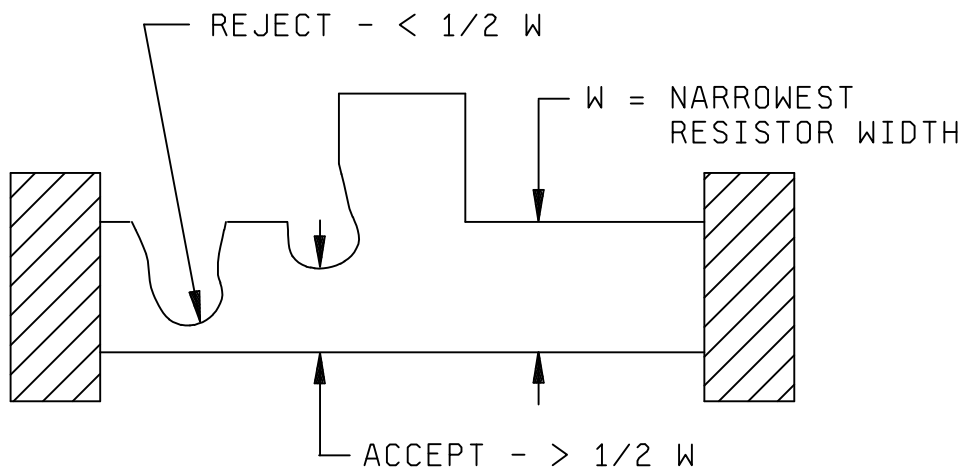


FIGURE 2010-29. Scratch and void criteria for untrimmed resistors.

- h. Any sharp change in color of resistor material within 0.1 mil of the resistor/connector termination.

3.1.7 Laser-trimmed thin-film resistors. Rejection shall be based on defects found within the actively used portions of the film resistor. No device shall be acceptable that exhibits:

- a. A kerf less than 0.1 mil in width, unless by design.

NOTE: Criteria does not apply for edge trimming.

- b. A kerf containing particles of detritus.

Condition A  
Class level S

Condition B  
Class level B

- c. A kerf containing untrimmed resistor material, unless that material is continuous across the kerf, and is undisturbed for a width greater than one-half times the narrowest resistor width, unless by design (see figure 2010-30).

NOTE: Maximum allowable current density requirements shall not be exceeded.

Top hat trim

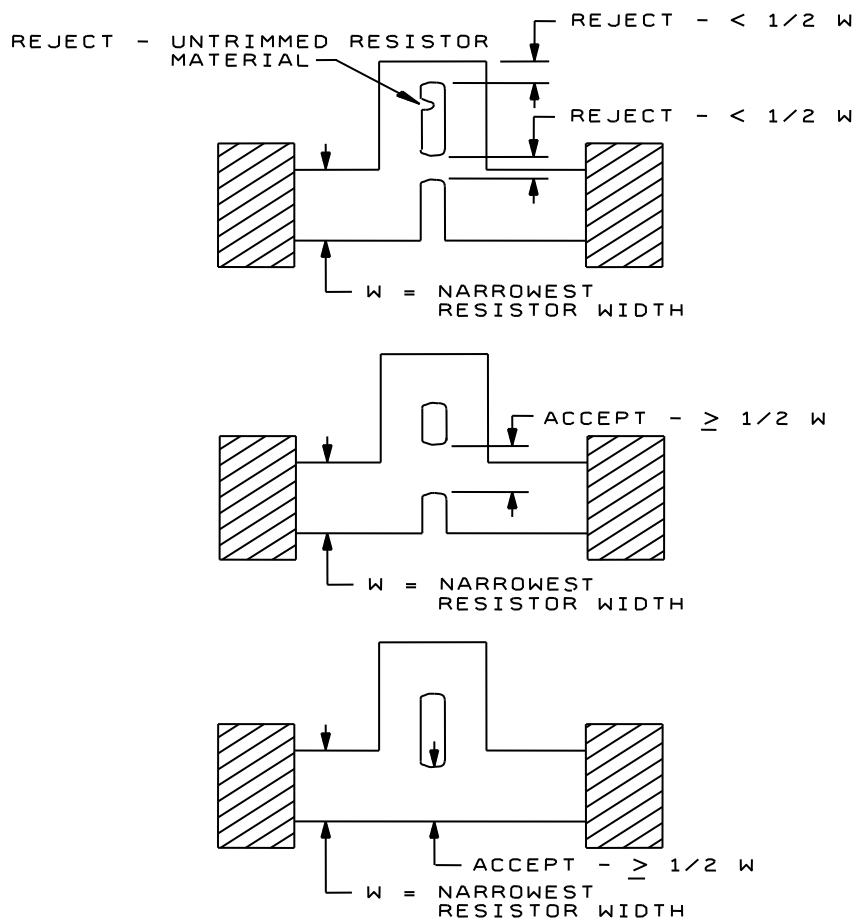
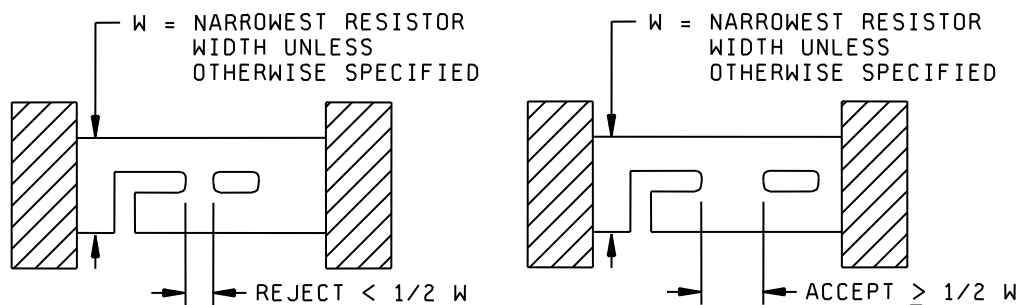


FIGURE 2010-30. Resistor Criteria.

Condition A  
Class level S

Condition B  
Class level B



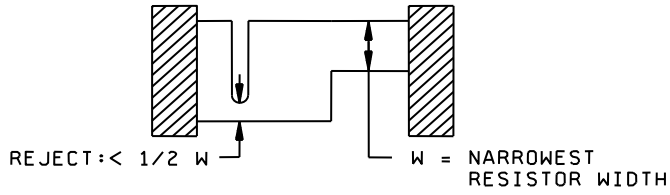
Rectangular L trim

FIGURE 2010-30. Resistor Criteria - Continued.

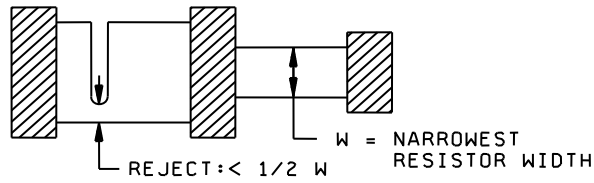
- d. Resistor width that has been reduced by trimming to less than one-half the narrowest resistor width, including voids, scratches, or a combination thereof, in the trim area (see figure 2010-31).

NOTE: Trimming of more than 50 percent of a given resistor shunt link is acceptable by design providing that the last shunt link of the resistor adder network is not trimmed greater than 50 percent. All trimmable resistor shunt links shall be defined on the design layout drawing.

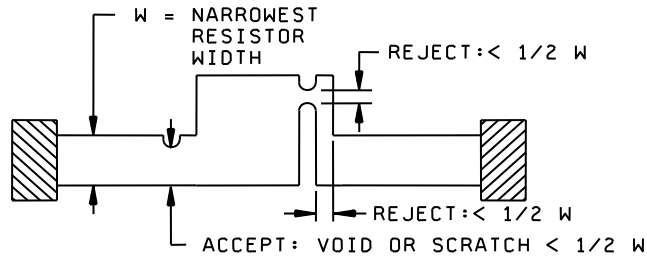




TWO RESISTORS IN SERIES WITH SAME  
CURRENT FLOWING THROUGH BOTH

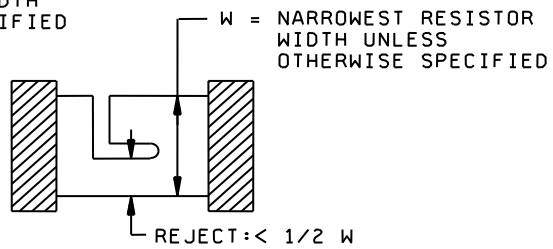
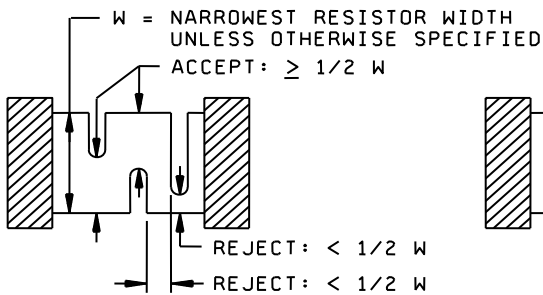


TOP HAT TRIM



SERPENTINE TRIM

RECTANGULAR L TRIM



Condition A  
Class level S

Condition B  
Class level B

- e. Trim path into the metallization except block resistors.

NOTE: This criteria can be excluded for trim paths into terminator ends of metallization runs. Conductors or resistors may be trimmed open for link trims or by design.

- f. Trim for block resistors which extends into the metallization (excluding bonding pads) more than 25 percent of the original metal width (see figure 2010-32).

TRIM INTO METAL

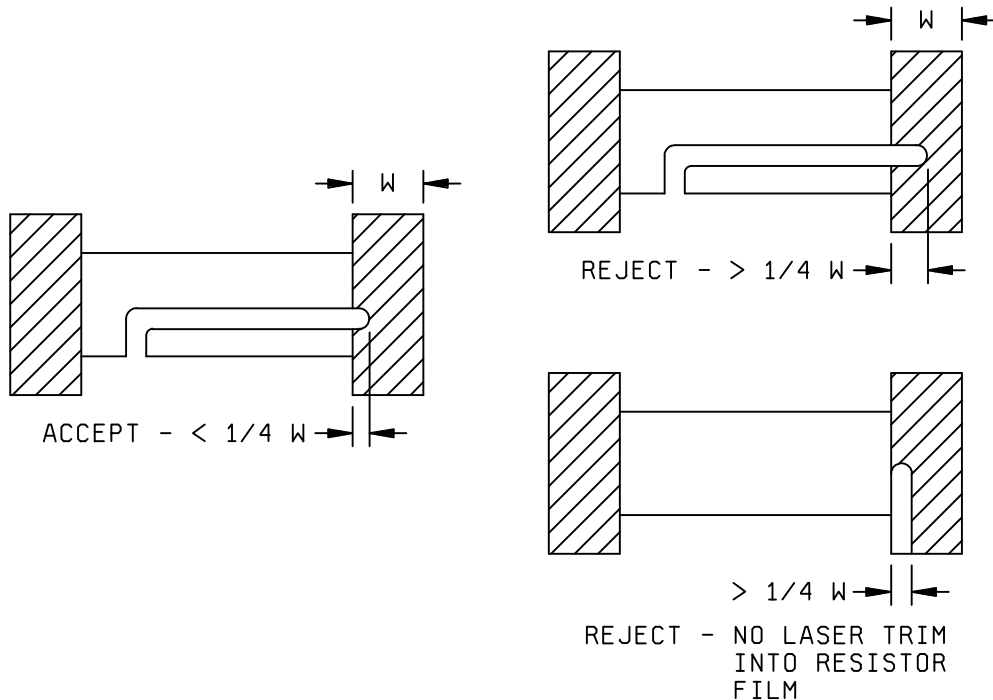


FIGURE 2010-32. Block resistor criteria.

- g. Pits into the silicon dioxide in the kerf which do not exhibit a line of separation between the pit and the resistor material.

Condition A  
Class level S

Condition B  
Class level B

3.2 Low power inspection. Internal visual examination as required in 3.2.1 through 3.2.3 shall be conducted on each microcircuit at low magnification range of 30X to 60X. In addition, the applicable criteria contained in 3.2.4 shall be applicable where beam lead assembly technology is used and 3.2.5 shall be inspected at both high and low power as indicated, high power magnification shall be same as 3.1, subject to conditions in 3b.

3.2.1 Lower power wire bond inspection. This inspection and criteria shall be required inspection for the bond type (s) and location(s) to which they are applicable when viewed from above (see figure 2010-33).

NOTE: The criteria applicable for bonds (called "wedgebonds" or "bonds") in this test method refers to the fully or partially deformed area including the tool impression shown as "L and W" in figure. The criteria applicable for "bond tails" (or "tails") in this test method refers to resulting length of bonding wire extending beyond the bond shown as "T" in figure 2010-33. Tail is not part of bond.

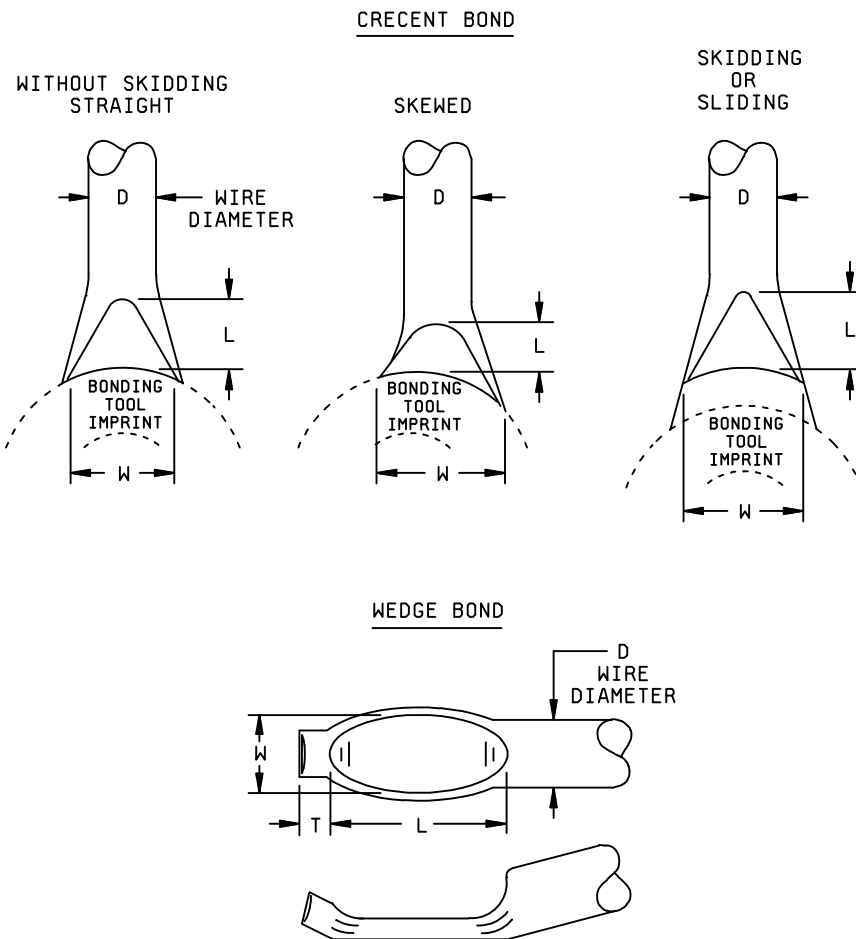


FIGURE 2010-33. Bond dimensions.

Condition A  
Class level S

Condition B  
Class level B

3.2.1.1 Gold ball bonds. No devices shall be acceptable that exhibits:

- a. Gold ball bonds on the die or package post wherein the ball bond diameter is less than 2.0 times or greater than 5.0 times the wire diameter.
- b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.
- c. Gold ball bonds where the wire center exit is not within the boundaries of the unglassivated bonding pad area.

3.2.1.2 Wedge bonds. No device shall be acceptable that exhibits:

- a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or more than 3.0 times the wire diameter in width, or less than 1.5 times or more than 6.0 times the wire diameter in length.
- b. Thermosonic wedge bonds on the die or package post that are less than 1.5 times or more than 3.0 times the wire diameter in width or are less than 1.5 times or more than 6.0 times the wire diameter in length.
- c. Bond width less than 1.0 times the wire diameter for aluminum wires 2.0 mils or greater in diameter.
- d. Wedge bonds where the tool impression does not cover the entire width of the wire.

3.2.1.3 Tailless bonds (crescent, terminating capillary bond). No device shall be acceptable that exhibits:

- a. Tailless bonds on the die or package post that are less than 1.2 times or more than 5.0 times the wire diameter in width, or are less than 0.5 times or more than 3.0 times the wire diameter in length.
- b. Tailless bonds where tool impression does not cover the entire width of the wire.

Condition A  
Class level S

Condition B  
Class level B

3.2.1.4 General (gold ball, wedge, and tailless). As viewed from above, no device shall be acceptable the exhibits (see figure 2010-16):

- |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>a. Bonds on the die where less than 75 percent of the bond is within the unglassivated bonding pad area.</p> <p>b. Bond tails that do not exhibit a line of separation between the tail and unglassivated metallization, another wire, wire bond, or wire bond tail, excluding common conductors and pads.</p> <p>c. Bond tails extending over glassivated metallization where the glass exhibits evidence of crazing or cracking that extends under the tail, excluding common conductors.</p> <p>d. Wire bond tails: Tails that exceed 2 wire diameters in length on die or on post.</p> <p>e. Bonds that are not completely within the boundaries of the package post. For glass sealed packages, bonds not within 20 mils of the end of post.</p> <p>f. Bonds (excluding bond tails) placed so that the horizontal distance between the bond and glassivated or unglassivated noncommon metallization, scribe lines, another bonding wire or bond is less than .25 mils.</p> | <p>a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.</p> <p>f. Bonds (excluding bond tails) placed so that the horizontal distance between the bond and glassivated or unglassivated noncommon metallization, scribe lines, another bonding wire or bond does not exhibit a visible line of separation.</p> |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

NOTE: When by design, there are multiple bonds on a common bonding pad or post they may not reduce the width of an adjacent bond by more than 25 percent.

NOTE: For SOS devices, exclude the insulator scribe lines.

- g. Bonds (excluding tails) placed such that less than 2.0 mils of bond periphery (on glassivated or unglassivated areas) is exposed to an undisturbed die metallization connecting path to/from the entering/exiting metallization stripe (see figure 2010-34).

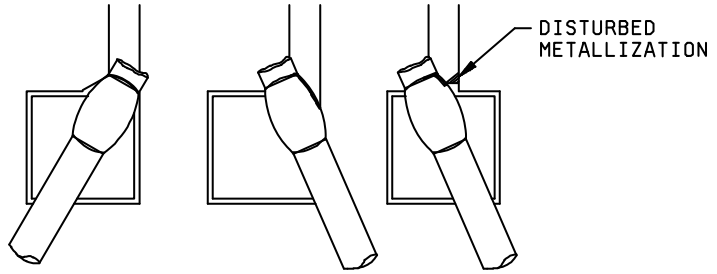
NOTE 1: When bond tails prevent visibility of the connecting path and the metallization immediately adjacent to the bond tail is disturbed, the device shall be unacceptable.

NOTE 2: When a fillet area exists, it is to be considered as part of the entering/exiting metallization stripe.

NOTE 3: This criteria is in addition to the bond placement criteria in 3.2.1.4a.

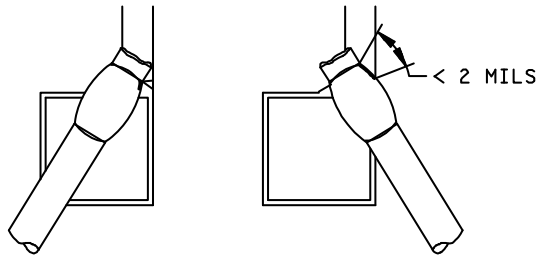
Condition A  
Class level S

Reject: Bond (excluding tails) placed, such that less than 2.0 mils of bond periphery (on glassivated or unglassivated areas) is exposed by an undisturbed die metallization connecting path to/from the entering/exiting metallization stripe.

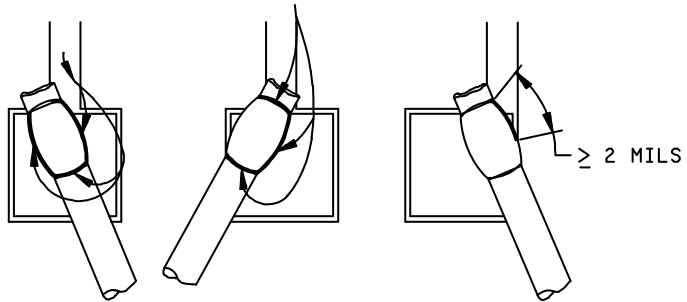


Condition B  
Class level B

Reject: When bond tails prevent visibility of the connecting path to the bond periphery and the metallization immediately adjacent to the bond tail is disturbed.



Accept: Bonds (excluding tails) placed, such that there is 2.0 mils or greater of bond periphery (on glassivated or unglassivated areas) exposed by an undisturbed die metallization connecting path to/from the entering/exiting metallization stripe.



Arrows demonstrate the connecting path to the bond periphery.

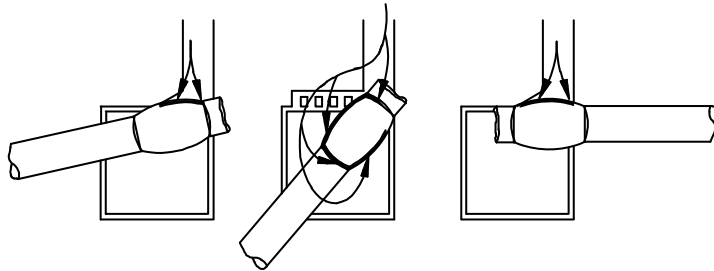


FIGURE 2010-34. Bonds at entering/exiting metallization stripe.

Condition A  
Class level S

Condition B  
Class level B

- h. Bonds where more than 25 percent of the bond is located on die mounting material.
- i. Any evidence of repair of conductors by bridging with additional material.
- j. Bonds on foreign material.
- k. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of that portion of the gold bond located on metal.

3.2.1.5 Rebonding of monolithic devices. Rebonding of monolithic microcircuits, may be done with the following limitations. No device shall be acceptable that exhibits:

- a. Rebond over exposed passivation or over metal which shows evidence of peeling. More than one rebond attempt at any design bond location. Rebonds that touch an area of exposed oxide caused by lifted metal.
- b. A bond on top of, or partially on top of, another bond, bond wire tail, or residual segment of wire.
- b. Bond along side or partially on top of another bond, bond wire tail or residual segment of wire, when the overlap width is greater than 25 percent.
- c. Rebond attempts that exceed 10 percent of the total number of bonds in the microcircuit. (e.g., for a 28 lead wire bonded package there are 56 bonds. A bond of one end of a wire shall count as a single attempt. A replacement of a wire bonded at both ends, counts as two rebond attempts.)

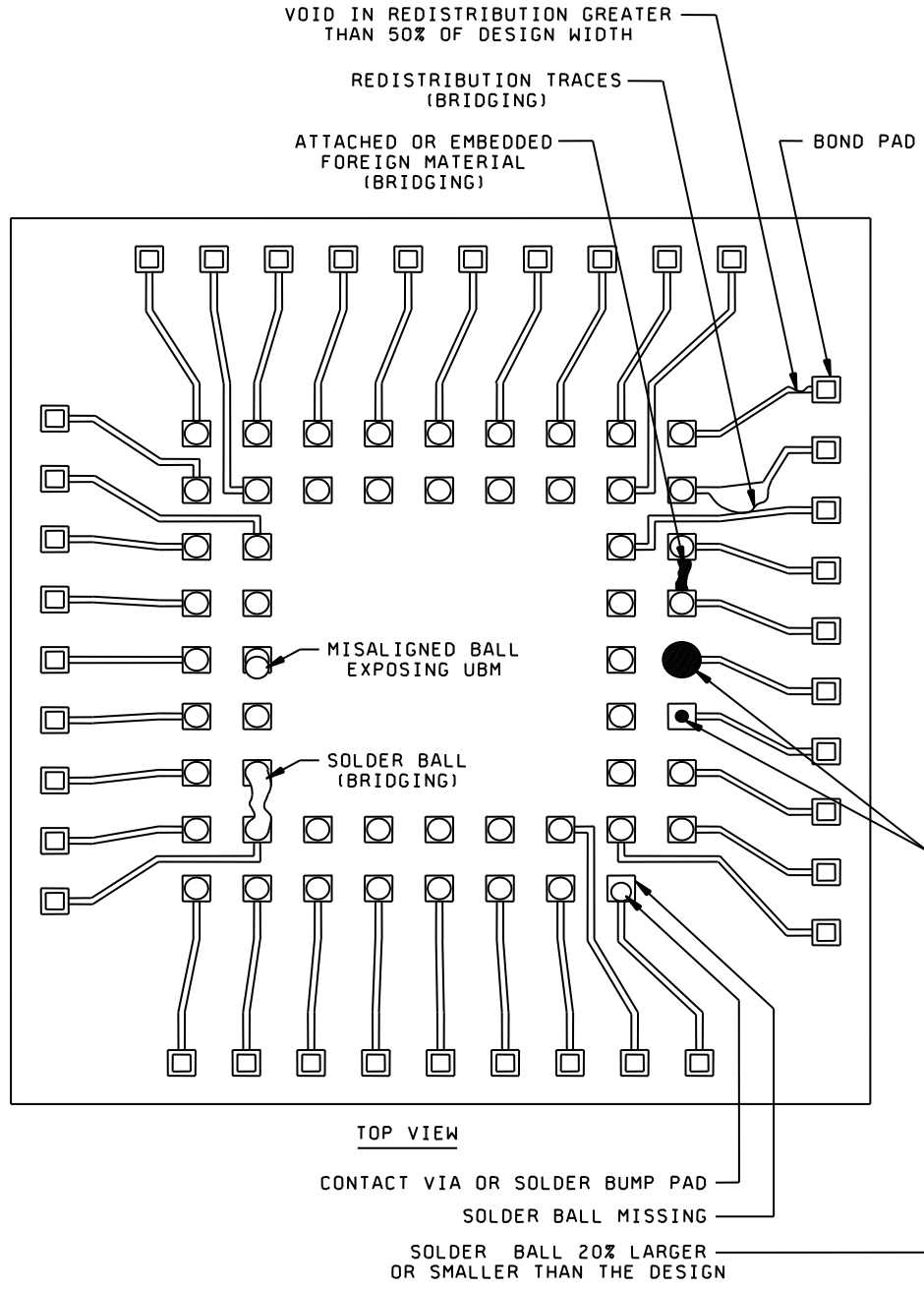
NOTE: For class level B only. Bond-offs required to clear the bond after an unsuccessful first bond attempt are not considered as rebonds provided they can be identified as bond-offs.

- d. Missing or extra wires.

3.2.1.6 Flip chip solder bump die. No solder bumped die shall be acceptable that exhibit any of the following characteristics (see figure 2010-34A):

- a. missing solder ball from original design position.
- b. Solder ball 20% smaller, or larger than design size (nominal).
- c. Solder balls bridging.
- d. Any attached or embedded foreign material bridging balls, or redistribution metalization.
- e. Misaligned solder ball which exposes the UBM on the contact via.
- f. Voids in redistribution metalization greater than 50% of the design width.
- g. Any redistribution metalization bridging.
- h. Any residual unetched UBM bridging balls or redistribution metalization.
- i. Mechanical damage to the ball which reduces the original height or diameter more than 20%.
- j. Lifting, or peeling or the RDL or dielectric material.

Note: Minor damage to the solder ball and bump misalignment can be reworked by performing a re-flow/refresh of the solder balls.





Condition A  
Class level S

Condition B  
Class level B

3.2.2 Internal wires. During inspection for the requirements of 3.2.2, each device shall be viewed at any angle necessary to determine full compliance to this specification, without damaging the device. No device shall be acceptable that exhibits:

- a. Any wire with a separation of less than two wire diameters to unglassivated operating metal, other bonds, another wire (common wires excluded), other package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any portion of the package including the plane of the lid to be attached.

NOTE: For condition A only. Within a 5.0 mil radial distance from the perimeter of the bond on the die the separation shall be 1.0 mil minimum.

- a. Any wire with a separation of less than one wire diameter to unglassivated operating metal, other bonds, another wire (common wires excluded), other package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any conductive portion of the package or the plane of the lid to be attached.

NOTE: For condition B only. Within a 10.0 mil radial distance from the perimeter of the bond on the die a line of separation must be visible.

NOTE: For SOS devices, exclude the unglassivated insulator areas.

- b. Nicks, bends, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.
- c. Tearing at the junction of the wire and bond.
- d. Any wire making a straight line run from a die bonding pad to a package post that has no arc.

Condition A  
Class level S

- e. Wire(s) crossing wire(s) when viewed from above, (excluding common conductors) except in multitiered packages, where the crossing occurs within the boundary of the lower wire bond tier(s) being crossed or packages with down bond(s). In these situations, the wires that cross are acceptable if they maintain a minimum clearance of two wire diameters (see figure 2010-35).

NOTE: No bond wire shall cross more than one other bond wire and there shall be no more than 4 crossovers or crossovers involving more than 10 percent of the total number of wires, whichever is greater for any single package cavity.

- f. Wire(s) not in accordance with bonding diagram.

3.2.3 Die mounting.

3.2.3.1 Die mounting eutectic. No device shall be acceptable that exhibits:

- a. Die mounting material buildup that extends onto the top surface or extends vertically above the top surface of the die.
- b. Die mounting material (eutectic wetting) not visible around at least two complete sides or 75 percent of the die perimeter, except for transparent die.
- c. Transparent die with less than 50 percent of the area bonded.
- d. Flaking of the die mounting material.
- e. Balling or buildup of the die mounting material that does not exhibit a minimum of 50 percent peripheral fillet when viewed from above or the accumulation of die mounting material is such that the height of the accumulation is greater than the longest base dimension or the accumulation necks down at any point (see figure 2010-36).

Condition B  
Class level B

- e. Wire(s) crossing wire(s) when viewed from above, (excluding common conductors) except that wires crossing wires bonded to package posts that are at difference heights, or wires bonded into the package cavity that cross are acceptable if they maintain a minimum clearance of two wire diameters (e.g., multitiered packages or packages with down bond chips).

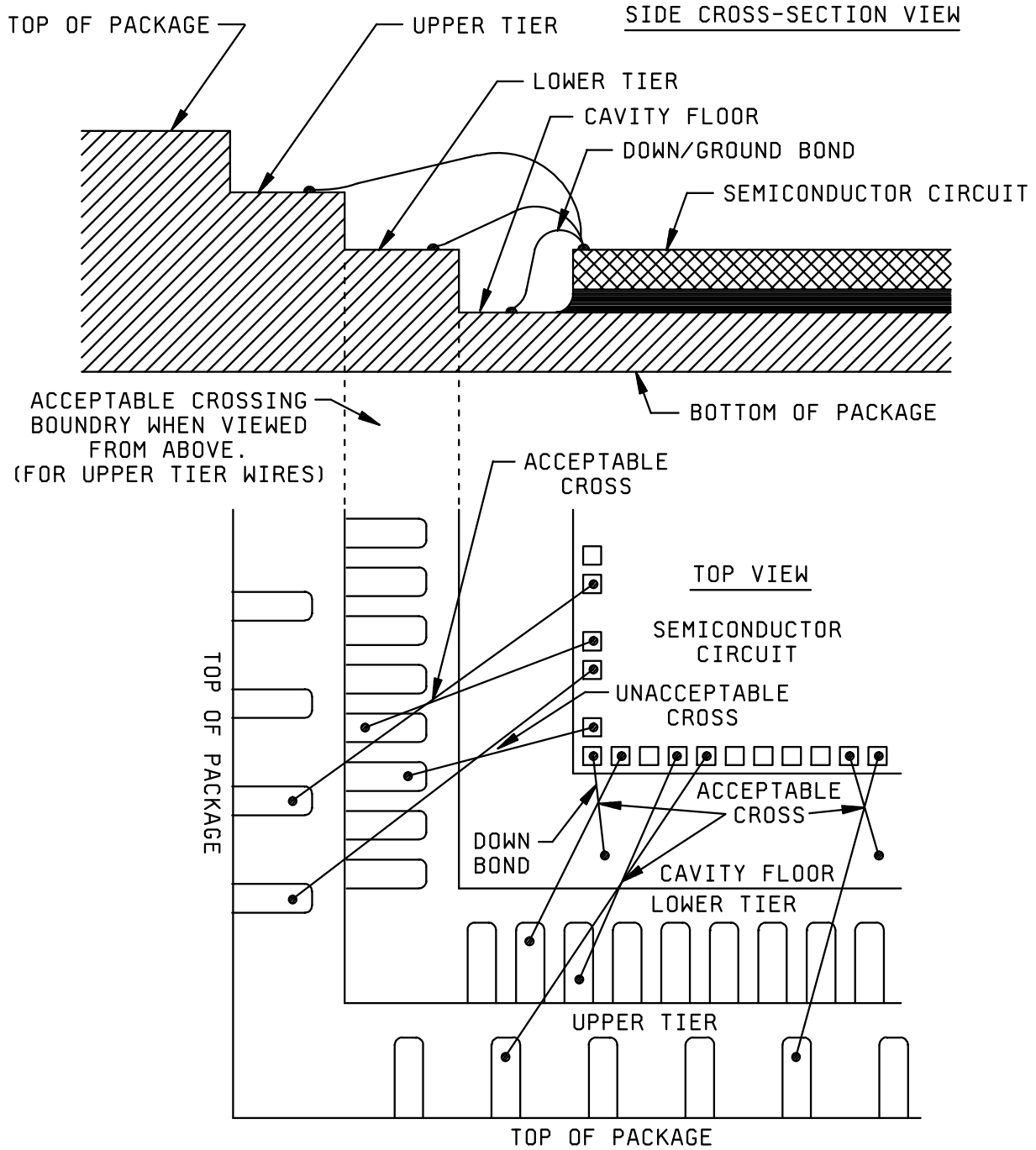
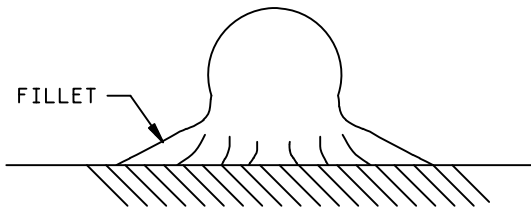
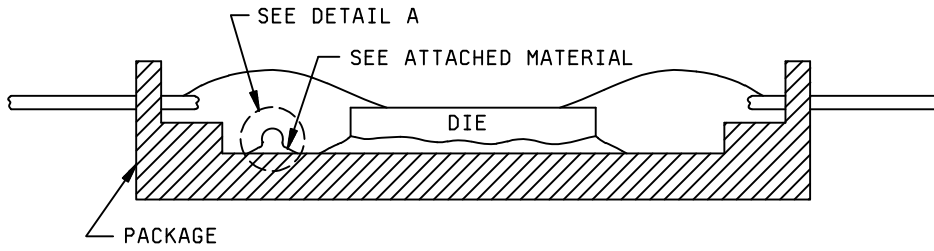


FIGURE 2010-35. Class level S criteria for wire(s) crossing wire(s).



DETAIL A  
FRONT VIEW, ACCEPT

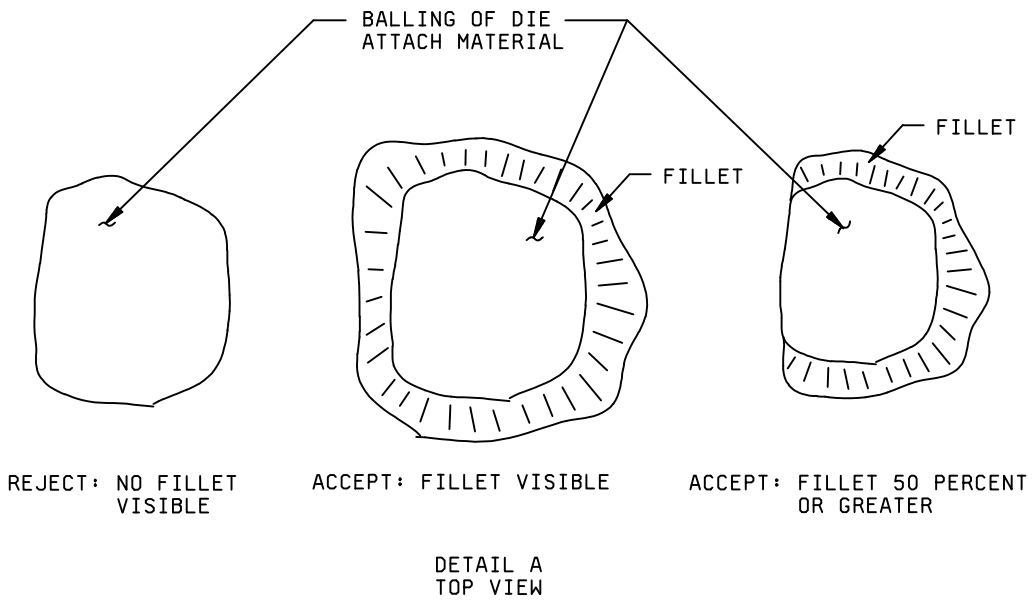


FIGURE 2010-36. Balling of die attach material.

Condition A  
Class level S

Condition B  
Class level B

3.2.3.2 Die mounting noneutectic. No device shall be acceptable that exhibits:

- a. Adhesive material immediately adjacent to the die that extends onto or vertically above the top surface of the die.
- b. Adhesive fillet not visible along 75 percent of each side of the die.
- c. Any flaking, peeling, or lifting of the adhesive material.
- d. Separation, cracks, or fissures greater than or equal to 2 mils in width in the adhesive at the cavity wall or cavity floor.
- e. Cracking in the adhesive.
- f. Adhesive that bridges package posts or is on the post bond area.
- g. Any adhesive material that is connected to the fillet or conductive cavity (e.g. metal package base or metallized floor of ceramic package), and extends up the cavity wall to within 1.0 mil of the package post.
- h. Transparent die with less than 50 percent of the area bonded.

3.2.3.3 Die orientation. No device shall be acceptable that exhibits:

- a. Die not located or oriented in accordance with the applicable assembly drawing.
- b. Die that appears to be obviously tilted (i.e., more than 10 degrees) with respect to the package cavity.

3.2.4 Beam lead construction.

3.2.4.1 Bonds. This inspection criteria shall apply to the completed bond area made, using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits:

- a. Bonds where the tool impression does not completely cross the entire beam width.
- b. Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15 percent (10 percent for compliant bonds) or greater than 75 percent of the undeformed beam width.
- c. Bonds where the tool impression length is less than 1.0 mil (see figure 2010-37).
- d. Bonding tool impression less than 1.0 mil from the die edge (see figure 2010-37).

Condition A  
Class level S

Condition B  
Class level B

- e. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned beam (see figure 2010-37).

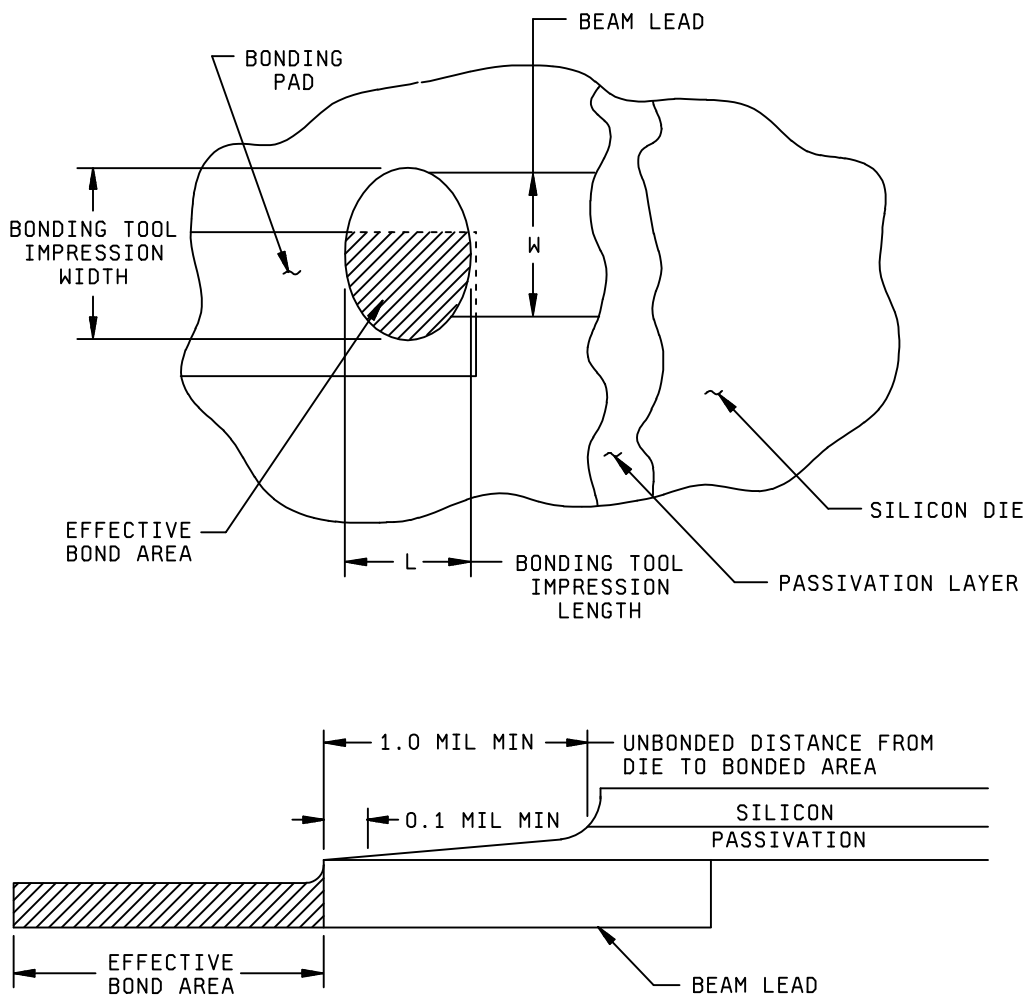


FIGURE 2010-37. Beam lead bond area and location.

Condition A  
Class level S

Condition B  
Class level B

- f. Cracks or tears in the effective bonded area of the beam greater than 50 percent of the original beam width.
- g. Bonds placed so that the separation between bonds and between bonds and operating metallization not connected to them is less than 0.1 mil.
- h. Bonds lifting or peeling.

3.2.4.2 Beam leads. No device shall be acceptable that exhibits the following:

- a. Voids, nicks, depressions, or scratches that leave less than 50 percent of the beam width undisturbed.
- b. Beam separation from the die.
- c. Missing or partially fabricated beam leads unless by design.
- d. Beam leads that are not bonded.
- e. Bonded area closer than 0.1 mil to the edge of the passivation layer.
- f. Less than 0.1 mil passivation layer between the die and the beam visible at both edges of the beam (see figure 2010-37 and 2010-38).

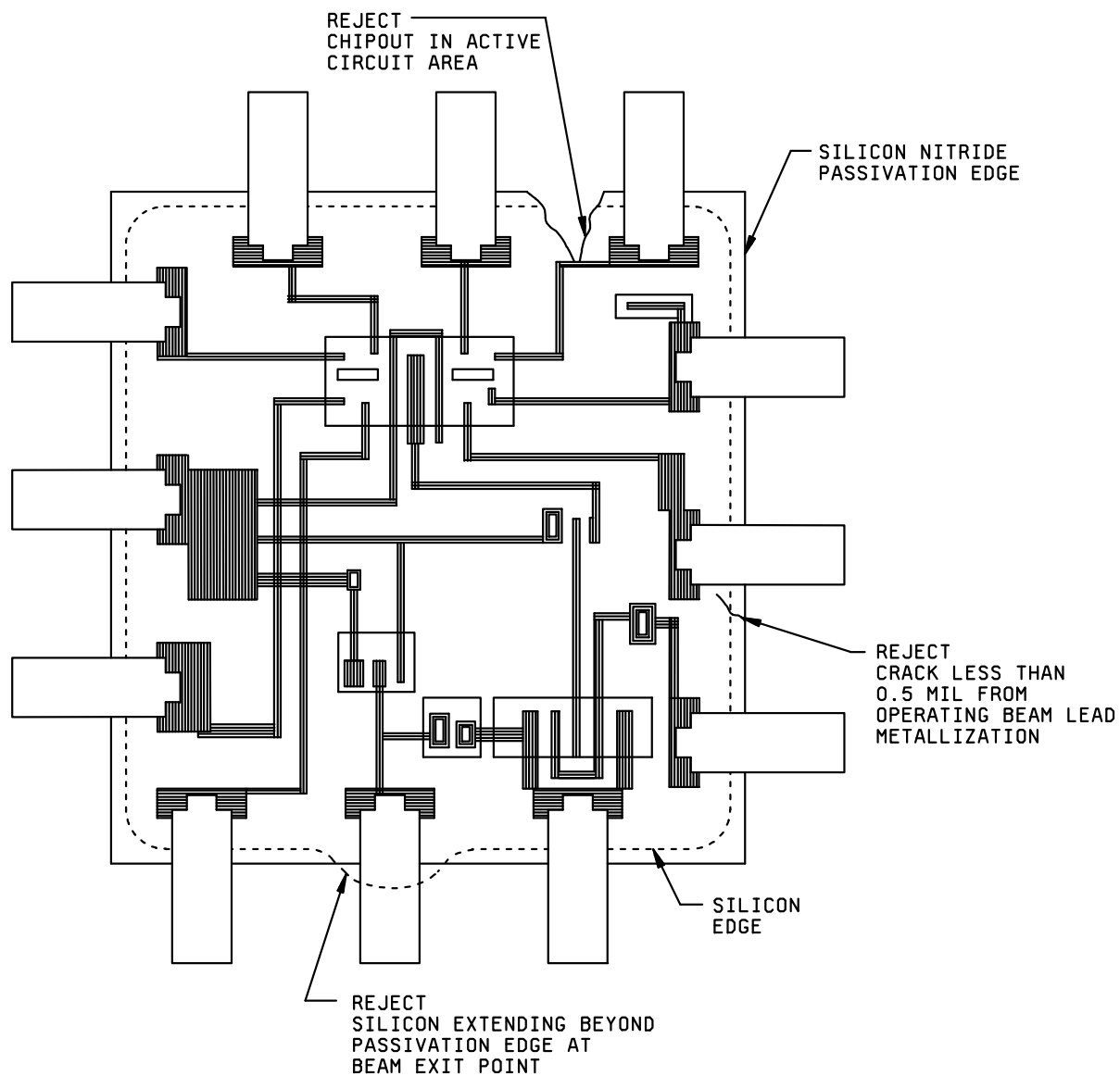


FIGURE 2010-38. Beam lead die faults.



Condition A  
Class level S

Condition B  
Class level B

3.2.5 Foreign material. Die inspections shall be at high magnification. Package and lid inspections shall be at low magnification. Die criteria may be examined at high magnification prior to die mounting provided they are re-examined at low magnification during preseat inspection. No device shall be acceptable that exhibits:

NOTE: Foreign material may be removed, if possible, by subjecting the device to a nominal gas blow (less than 25 psig). After this gas blow off at inspection, all wire bonded devices shall be inspected/reinspected for possible wire damage. Use of a higher psig value is permitted provided that the manufacturer has characterized the process and has data to assure that no damage is done to the wire bonds. This data shall be available upon request to the preparing or acquiring activities.

- a. Foreign particle(s) on the surface of the die that is (are) large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.).
- b. Foreign particle(s) other than on the surface of the die within the package or on the lid or cap that is (are) large enough to bridge the narrowest spacing between unglassivated operating materials and are not the following: Semiconductor material, glass splatter, gold imperfections in the die attach area, gold eutectic material or package ceramic material.

NOTE: As an alternative to 100 percent visual inspection of lids or caps, the lids or caps may be subjected to a suitable cleaning process and quality verification, approved by the qualifying activity. The lids or caps shall subsequently be held in a controlled environment until capping or preparation for seal.

- c. Foreign material attached to or embedded in the die surface that appears to bridge the active circuit elements including metallization unless verified as only attached but not embedded by high power dark field illumination.
- d. Liquid droplets, chemical stains, ink, or photoresist on the die surface that appear to bridge any combination of unglassivated metallization or bare semiconductor material areas.
- e. A particle of gold eutectic material, package ceramic material or semiconductor material, not attached to the die, large enough to bridge the narrowest spacing between unglassivated operating materials, that does not exhibit a minimum of 50 percent cumulative peripheral fillet or whose height is greater than the longest base dimension.

NOTE 1: This criteria shall not be cause for rejection when the assembly process contains a gas blow (less than 60 psig) after die attach and again (less than 25 psig) after wire bond provided rejectable materials (not attached and large enough to bridge) have been removed from the cavity.

NOTE 2: Gold imperfections in the die attach area that do not interfere with proper die attachment, sealing glass splatter (provided it does not suggest inadequately controlled process and does not interfere with the die attach area) or internal glass run out from frit seal (provided it is confined to package walls and does not interfere with the die attach area) are not rejectable.

Condition A  
Class level S

Condition B  
Class level B

3.2.5.1 Foreign material, die coated devices. This inspection and criteria shall be required on all devices that receive a die coat during the assembly process. This inspection will be done after die coat cure. No device shall be acceptable that exhibits:

- a. Unattached foreign particles on the surface of the die coat or within the package that is (are) large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.). Note: Semiconductor particles shall be considered as foreign material.
- b. Partially embedded foreign material with an "unembedded portion" that is large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.).
- c. Foreign material attached to or embedded in the die coat that appears to bridge unglassivated operating material when viewed from above (e.g., bare semiconductor material, bond pads, bonding wire, mounting material, etc.).
- d. Embedded foreign particles that penetrate the entire thickness of the die coating.

3.2.5.1.1 Die coating material. No device shall be accepted that exhibits:

- a. Surface scratches that penetrate the die coating and expose underlying glassivated metal.
- b. Die coating that is lifted or is peeling from the semiconductor surface.

3.2.6 GaAs backside metallization. GaAs inspection shall be performed with low magnification prior to die mounting. (Verification at high magnification is permitted.) With the approval of the acquiring activity, the manufacturer may substitute a sample inspection plan at the wafer level for 100 percent inspection in dice form. The sample inspection plan shall be documented in the manufacturer's baseline documentation and shall be performed to the requirements of test method 5013. No devices shall be acceptable that exhibit the following.

- a. Evidence of metal corrosion, lifting, peeling, blistering.
- b. Voids or scratches that expose underlying metal or substrate whose cumulative areas are more than 25 percent of the cell area or device area.  

NOTE: Absence of gold in the die separation area (saw street) of devices with electroplated backside metallization is not a cause for rejection. Small voids at edges due to die separation are acceptable if they comprise less than 10 percent of the backside area.

- c. Any voids or scratches in the substrate via metallization that effects more than 25 percent of the metallization or cause unintended isolation of the metallization path.
- d. Underetched vias.
- e. Overetched vias.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

- a. Test condition (see 3).
- b. Where applicable, any conflicts with approved circuit design topology or construction.
- c. Where applicable, gauges, drawings, and photographs that are to be used as standards for operator comparison (see 2).
- d. Where applicable, specific magnification (see 3).